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Nanopatterning Technologies of 2D Materials for Integrated Electronic and Optoelectronic Devices

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With the reduction of feature size and increase of integration density, traditional 3D semiconductors are unable to meet the future requirements of chip integration. The current semiconductor fabrication technologies are approaching their physical limits based on Moore's law. 2D materials such as graphene, transitional metal dichalcogenides, etc., are of great promise for future memory, logic, and photonic devices due to their unique and excellent properties. To prompt 2D materials and devices from the laboratory research stage to the industrial integrated circuit-level, it is necessary to develop advanced nanopatterning methods to obtain high-quality, wafer-scale, and patterned 2D products. Herein, the recent development of nanopatterning technologies, particularly toward realizing large-scale practical application of 2D materials is reviewed. Based on the technological progress, the unique requirement and advances of the 2D integration process for logic, memory, and optoelectronic devices are further summarized. Finally, the opportunities and challenges of nanopatterning technologies of 2D materials for future integrated chip devices are prospected.

1. Introduction

The successful application of nanofabrication technologies in traditional semiconductor materials (e.g., Si, GaAs, GaN, etc.) is the main building block for producing current integrated circuit (IC)-based chips.[1,2] To integrate various electric components into a chip, controllable nanopatterning of the semiconductor materials is usually a critical prerequisite.[3,4] Nanopatterning technologies for silicon have developed to sub-10 nm, and the number of transistors on a chip has been following the Moore's Law.[5–8] However, when the feature size of transistors is close to the physical limit, short-channel effects cause sharp performance degradation.[9–14] Therefore, various new materials have been constantly exploited for future electronic and optoelectronic devices with ultrahigh integration density. Over the past decades, various novel material systems such as organic polymers,[15] perovskite,[16] and carbon nanotubes (CNTs)[17,18] have been reported. Recently, the emerging 2D layered van der Waals (vdW) materials such as graphene and transitional metal dichalcogenides (TMDs) have received extensive research interests due to their unique physical properties, making them promising candidates for the future chip industry to prolong Moore's law.[19–23] To realize the practical application, the controllable synthesis and subsequent nanopatterning of 2D materials are of great importance and inevitably require extensive research exploration.[9,24–26]

Nanopatterning bridges the microstructure of 2D materials and the integrated electronic and optoelectronic chips, essentially enabling and prompting their successful application in industry.[27–30] Albeit traditional nanopatterning processes have been mostly focused on silicon-based manufacturing, researchers recently start to pay more and more attention to develop novel nanopatterning techniques particularly regarding the structural requirement of 2D material.[31,32] Increasing research articles have been focused on the actual application of 2D materials for large-scale integrated devices.[33–41] This is expected to significantly prompt their industrialization progress in various electronic and optoelectronic device systems.[42–44] For example, the channel length of 2D materials has been decreased from micrometer scale to nanometer scale. Assisted by probe, sub-20 nm resolution is easy to achieve[45] and wafer-scale fabrication has been exploited.[46] It is noted that sub-1 nm vertical gate channel has successfully fabricated on a 2 in. wafer, significantly promoting the application of 2D materials.[47] Most recently, wafer-scale ICs with channel length of 5 μm has emerged. The fabrication process is close to the

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standard industrial process.[48] Along with advances of the key metrics in nanopatterning technologies, there are other new features such as contact resistance. By employing induced growth, lateral metal–TMD contact has been fabricated with low Schottky barrier (SB).[49] Also printing graphene electrodes avoids metal deposition and suppresses the interface defects.[50] All these advanced progresses have been barely touched in the previous reviews.

Besides, nanopattern of 2D materials helps to modulate the optical and electronic properties. First, light–matter interaction largely depends on the nanopattern of 2D materials. The wavelength of photons and mean electron path are important relevant length scales.[51] As a result, the optical properties are prominently modulated by the morphology of 2D materials. 1D MoS_2 exhibited photoluminescence (PL) 50 mV higher than in-planar 2D MoS_2.[52] Besides the modulated optical properties, 2D materials could be designed into various patterns to achieve different functions. For example, tunable localized plasmon could be achieved in metasurface made from patterned graphene.[53] The metasurface could be designed to interact with wide frequency range terahertz wave (0.1–2.0 THz).[53] Also, optical properties could be modulated by the strain which could be introduced via patterns on the substrates. For example, the photoresponse of MoS_2/graphene junctions could reach near-infrared regime induced by the strain.[54] Second, the emerging fabrication of 3D structure for 2D materials also has the potential to expand the application of it in memory and logic devices. For example, the wrinkled MoS_2 exhibited excellent multilevel storage performance with on/off ration of 10^6 and retention time $>10^4$ s.[55] The wrinkles built in the MoS_2 could help to trap the carrier so as to promote the performance.[55]

Herein, we first summarize the most recent development of nanopatterning technologies for 2D materials, including the well-accepted bottom-up and top-down strategies, mainly focusing on their merits and drawbacks for practical device application. Based on the technological progress, we further summarize the unique requirement and advances of the 2D integration process for logic, memory, and optoelectronic devices. The key advances of the integrated devices such as the integration density, feature size, device-to-device variability, etc., have been summarized in this part. We also discussed how nanopatterning technologies affect the performance of these devices. Finally, based on our understanding, we prospect the opportunities and challenges of nanopatterning technologies for the nanofabrication of 2D materials in future integrated devices.

2. Nanopatterning Technologies for 2D Materials

As we noted above, nanopatterning technologies for 2D materials aim to promote their practical application toward the industrial scale.[56,57] Similar to the traditional semiconductor industry, the reported nanopatterning technologies for 2D materials can be generally divided into two categories: bottom-up methods and top-down methods.[3,4,58] In the bottom-up methods, nano-objects or various single units are constructed together to form microstructures via the interaction forces of atoms and molecules; while the top-down methods involve directly processing the macrosized 2D materials to nanopatterns based on the sophisticated lithography techniques and other advanced nanofabrication techniques.[3,58,59] The chief nanopatterning methods are illustrated in **Figure 1**. We critically focus on the conceptional and processing characteristics of various nanopatterning technologies in the following sections.

2.1. Bottom-Up Methods

2.1.1. Seeds-Induced Growth

Contemporarily, the high-quality and large-scale growth of patterned 2D materials is still challenging. During a typical chemical vapor deposition (CVD) process, the low nucleation barrier of 2D materials results in the inevitable formation of randomly distributed single crystals or polycrystalline films on the substrate, which makes the control of the microstructure (e.g., grain size, grain orientation, distribution of grain boundaries, etc.) of the products very difficult and severely hinders their large-area growth and patterning with high quality.[60–62] To overcome this problem, increasing the nucleation barrier has been the most effective method for the controllable growth of large-area 2D single crystals.[63,64] Consequently, it is of significance to precisely control the numbers and positions of the nucleus on a macrosized substrate to prevent unnecessary nucleation.[35,36,65]

The seeds-induced growth, in which the nucleus is artificially generated in a high nucleation barrier environment, has been pioneeringly proposed to solve this problem.[25,66] Precursors are placed in the specific positions on the substrates in a macro range by lithography or direct writing technologies. The CVD growth is then applied to realize the formation of 2D materials preferentially at the precursor locations (Figure 1a).[67–70] Also, it is possible to grow specific arrays and patterns of 2D materials by controlling the positions of seeds (Figure 1b). With such a manner, the seeded growth has been rapidly employed for various 2D materials including graphene, TMDs (e.g., MoS_2, WS_2, PtS_2, etc.). The seeds materials are in great diversity involving organic precursors, noble metals, and modified substrates.[35,41,52,71]

The theoretical calculation has proved that less active transition metal surfaces (e.g., Au, Pd, Cu, etc.) can induce the large-scale growth of graphene.[72–74] Following this mechanism, arrayed poly(methyl methacrylate) (PMMA) dots were patterned on Cu foil via electron beam lithography (EBL) to induce the growth of spatially ordered arrays of single-crystal graphene.[37] PMMA dots provide initial nucleus and generate high concentration carbon source region to suppress the nucleation of graphene. Similarly, Way et al. studied and engineered the seed-initiated growth of graphene nanoribbons on Ge (001) by using the prepatterned graphene as the seeds (**Figure 2**a).[75] Aluminum masks were employed to obtain graphene seeds array after hexogen graphene was initially fabricated. Graphene seeds determine the locations where the growth would occur and allow graphene to grow with lattice orientations that do not spontaneously form without seeds. Unlike graphene, whose lattice symmetry is sixfold, many 2D materials including h-BN

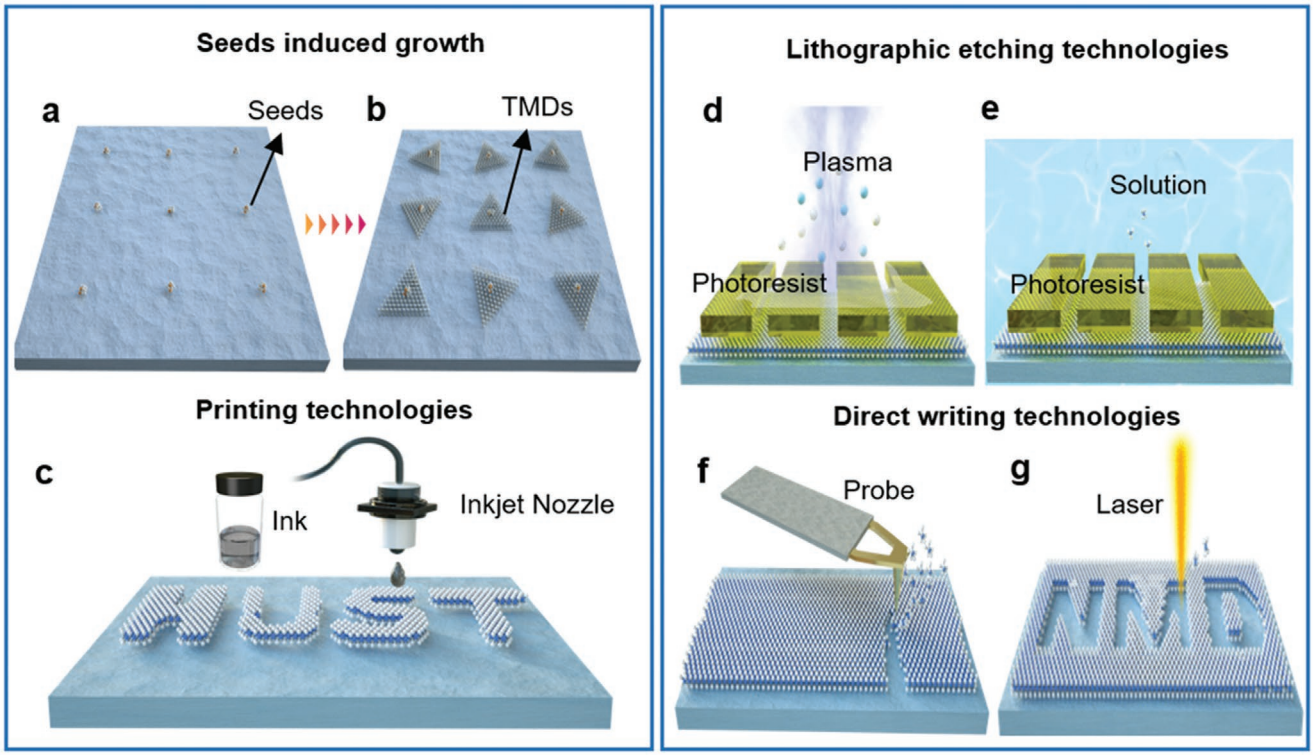

Figure 1. Nanopatterning technologies for 2D materials. a–c) Schematic of typical bottom-up methods including seeds-induced growth (a,b) and printing technologies (c). d–g) Schematic of typical top-down methods including lithography aided etching technologies such as reactive ion etching (d) and wet etching (e), and direct writing technologies such as probe processing (f) and laser processing (g). Note: "HUST" in (c) is the abbreviation of our home affiliation "Huazhong University of Science and Technology" and "NMD" in (g) is the abbreviation of our research group "Center of New Materials and Devices."

and most TMDs possess a threefold symmetrical structure, making lattice match between these 2D materials and the substrates more difficult.[76] With this consideration, Johnson et al. prepared patterned molybdenum sources in SiO_2/Si substrates for the growth of MoS_2 (Figure 2b). This work paves a new way to fabricate 2D materials in the specific patterns, but the corresponding mechanism was unrevealed yet in this study.[25]

Mechanism for the CVD growth of TMDs was initially found to be owing to its self-seeding fullerene nuclei.[77] Enlightened by such natural nucleation process, seeds such as Pt/Ti dots[71] and Au dots[78] have been put forward to serve as fullerene-like nucleus for the growth of TMDs. Li et al. prepared arrayed Au seeds for MoS_2 growth and proved that the Au seeds decreased formation energy of MoS_2 due to the lattice match between Au (111) surface and out-plane of MoS_2 through high-resolution transmission electron microscopy (HRTEM) and density function theory calculation. This study not only provides means for programmable and controllable synthesis of TMDs (Figure 2c), but also contributes to the understanding of the seeded-growth mechanism.[79] For instance, by combining Au-seeded growth with a confined area strategy, Mohapatra et al. successfully synthesized a large-area MoS_2 membrane with controlled microstructure afterward.[70]

In addition to Au seeds, specific modification of substrate was also employed to realize the MoS_2 array fabrication.[35] Ryu et al. applied 3D printer to fabricate triboelectric charge patterns on the dielectric substrates through rubbing process.[80] Rubbed SiO_2 area provides the nucleation sites for MoS_2 during the CVD process, resulting in successful in-site growth of patterned MoS_2. Besides the successful realization of seeded growth of MoS_2 patterns, nanopatterning of other TMDs, such as WS_2 (Figure 2d), WSe_2, etc., has also been prepared with similar seeding approaches for various electronic and optoelectronic devices.[78]

In situ transformation is another critical technology for the fabrication of large-area patterns of TMDs.[81,82] Precursors are directly patterned on substrates and then transformed into specific TMDs through chemical reactions. Compared to the direct printing of liquid-exfoliated 2D materials, preprinting precursors followed by conducting chemical conversion favor the formation of 2D nanopatterns with higher quality and larger crystal domains.[83,84] For instance, Lim et al. utilized the spin-coating method to print $(NH_4)_2MoS_4$ on SiO_2/Si substrates followed by a post-annealing to obtain few-layer MoS_2.[85] Recently, Wan et al. printed aqueous precursors of ammonium molybdate tetrahydrate $(NH_4)_6Mo_7O_{24}\cdot 4H_2O$ on the SiO_2/Si substrate (Figure 2e).[86] Specific patterns of precursors are facile to fabricate (Figure 2f). A rapid heating process was then implemented using a magnet to rapidly move the printed substrate into the heating zone in the temperatures range of 750 to 1050 °C. In this way, patterned MoS_2 and $MoSe_2$ were successfully synthesized (Figure 2g). The thickness of patterned 2D materials is controllable by manipulating the amount of precursors on the substrates. Additionally, patterned MoS_2/$MoSe_2$ vertical

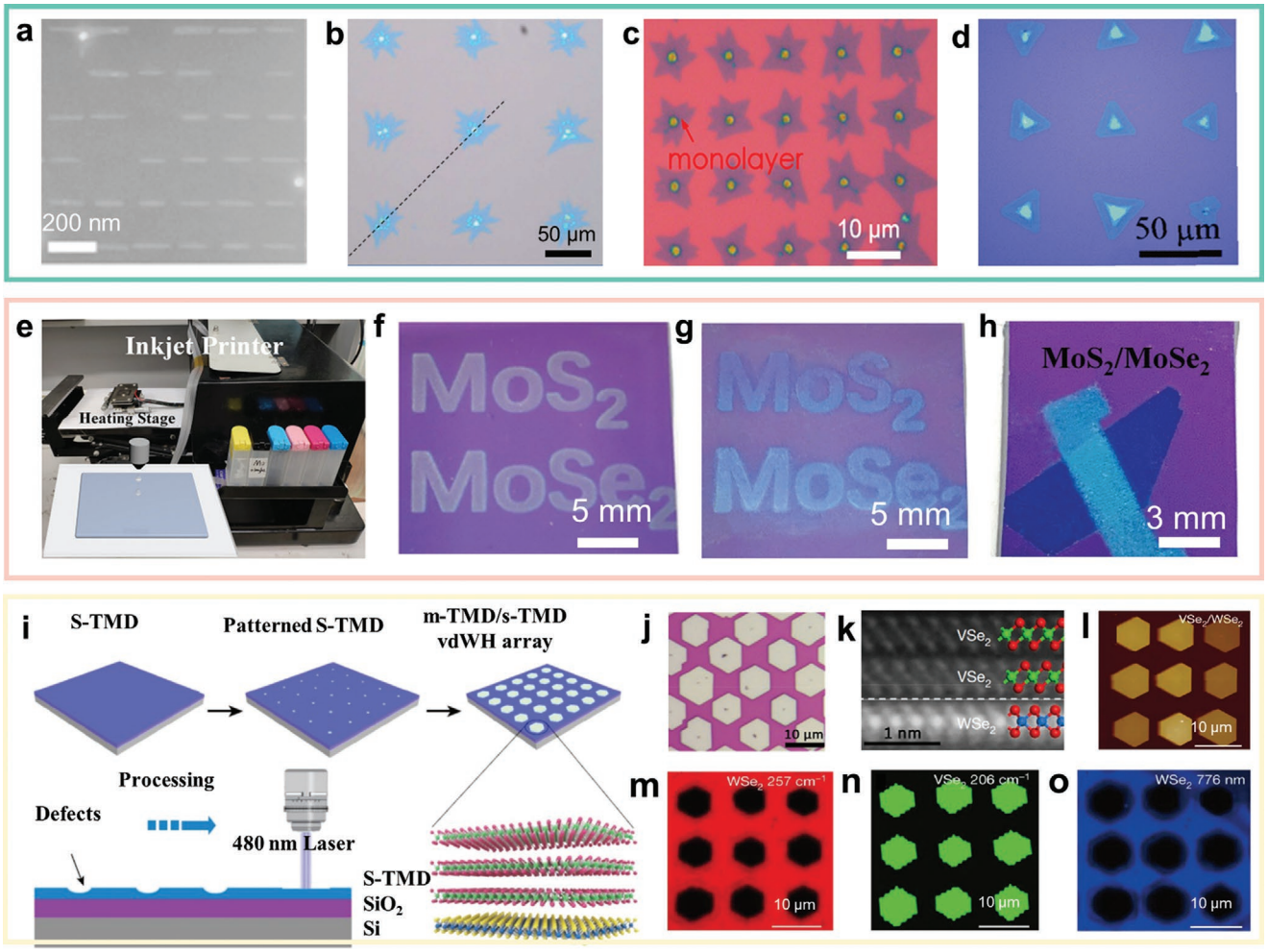

Figure 2. Seeds-induced growth technologies. a–d) Various 2D nanopatterns obtained by seeds-induced growth technologies: a) graphene nanoribbons; b) MoO_3-seeds-induced MoS_2 array; c) Au-seeds-induced MoS_2 array; d) Au-induced WS_2 array. Reproduced with permission.[75] Copyright 2018, American Chemical Society. b) Reproduced with permission.[25] Copyright 2015, Springer Nature. c) Reproduced with permission.[79] Copyright 2018, American Chemical Society. d) Reproduced with permission.[78] Copyright 2019, Royal Society of Chemistry. e) Set-up of inkjet printer used for the in situ transformation technology. f–h) Printed patterns of precursors (f) and the transformed final TMD patterns (g) and TMD heterostructure patterns (h). e–h) Reproduced with permission.[86] Copyright 2021, Wiley-VCH. i) Schematic illustration of the defect-induced growth of TMD heterostructures. j) The VSe_2/WSe_2 heterostructure arrays as well as their k) TEM image and l) AFM image. m,n) Raman mapping corresponding to WSe_2 (m) and VSe_2 (n). o) PL mapping corresponding to WSe_2. i–o) Reproduced with permission.[88] Copyright 2020, The Authors, published by Springer Nature.

heterojunctions are also obtained through this way (Figure 2h). In this work, $(NH_4)_6Mo_7O_{24}\cdot 4H_2O$ was chosen as the aqueous precursor due to its high solubility in water, low cost, high stability and safety in ambient, as well as its wide availability in industry.[86]

Moreover, the defect-induced growth strategies have also been well-developed for the controlled fabrication of patterned TMDs as well as their heterostructures.[87] Recently, Li et al. prepared a wafer-scale patterned 2D heterojunctions array by using the laser-created defects as the seeds.[88] As illustrated in Figure 2i, the authors first utilized laser to prepare defects on the semiconductor TMD (s-TMD) layer. The defective areas were further served as the nucleation sites for epitaxial growth of the second-layer metal TMD (m-TMD). With such a manner, various patterned 2D heterojunction arrays, such as VSe_2/WSe_2, $NiTe_2/WSe_2$, $CoTe_2/WSe_2$, and $NbTe_2/WSe_2$, are successfully fabricated. A typical optical image of the VSe_2/WSe_2 with highly oriented array structure is shown in Figure 2j. The m-TMD grows laterally after nucleation at laser-induced defects to eliminate lattice distortion since the vdW gap reduces interactions between s-TMD and m-TMD layers, which is proved by the HRTEM image (Figure 2k). The as-fabricated vdW heterojunction arrays exhibited high uniformity (Figure 2l). To confirm the vdW heterojunction arrays are formed with separated pure phase, Raman mapping images of peaks 257 and 206 cm^{-1} (corresponding to 2H WSe_2 and 1T VSe_2, respectively) are generated and clearly show the distinct spatial modulation (Figure 2m,n). The PL mapping of WSe_2 (Figure 2o) further demonstrates that the quality of WSe_2 substrate is largely retained during the growth of VSe_2.[88]

Overall, the seeds-induced growth has been widely applied for various 2D materials due to its convenience in processing,

good stability, and high universality. The whole production flow of 2D materials nanopatterns is facile to achieve.[25,78,79] The controllable fabrication flow ensures the high quality of the products. In addition, seeds could be designed depending on the different materials. In general, seeds-induced growth is suitable for wafer-scale fabrication.[88] Nevertheless, it is worth mentioning that the induced growth is not the panacea for all the desired 2D structures. First, the induced growth inevitably makes the formation of grain boundaries, which causes low electron mobility and suboptimal performance for electronic and optoelectronic devices.[76] Second, the seeds might contaminate the surface of 2D materials, making the nanopatterns sometimes not preferential for high-precision applications.[66] Last, it is tough to precisely control the orientation of as-grown 2D materials on an isotropy substrate through the induced growth, which is not beneficial for the devices to perform well consistently.[89] The typical feature size of 2D materials fabricated by induced growth ranges from one to hundreds μm. As a result, further nanofabrication techniques are often required to reshape the nanopatterns of 2D materials synthesized by the induced growth strategies.

2.1.2. Printing Technologies

Printing technologies for nanopatterns of 2D materials have been developed for more than 10 years, which is initially applied for graphene and has been prompted to a variety of 2D family such as TMDs, black phosphorus (BP), h-BN, and the newly emerging MXene materials (Figure 1c).[90] Printing technologies contain ink-jet printing, roll-to-roll printing, template-assisted printing, etc.[91–93] Contemporarily, inks such as dimethylformamide (DMF), *N*-methyl-2-pyrrolidone (NMP) are mostly used to disperse graphene or other 2D materials.[40] Direct graphene ink-jet printing patterns on flexible substrates were initially reported in 2011.[94] Fabrication of field effect transistors (FETs) through such ink-jet printing were further reported in 2012, with a highly controllable film thickness and an on/off ratio possibly reaching 4×10^5.[95] After that, more functional inks have been developed to improve the quality and production efficiency of 2D materials.[96,97] Besides their successful application in electronic and optoelectronic devices,[98,99] they are also widely used in other areas such as lithium battery electrodes[100] and microsupercapacitors. [101–103]

The solution-processed 2D TMD nanopatterns had thought to be difficult to apply in electronics and optoelectronics because of their poor performance in FETs caused by inevitable solution contaminations in early years.[98,104] To optimize the quality of printed TMDs, Lin et al. reported a general method to prepare highly uniform and pure-phase semiconductor nanosheets, for which tetraheptylammonium bromide (THAB) was first electrochemically embedded into the 2D crystals, followed by the gentle ultrasonic treatment and the peeling process.[105] By precisely manipulating the intercalation chemistry, pure 2H phase of MoS_2 nanosheets with a narrow thickness distribution was obtained. **Figure 3**a shows the THAB-exfoliated MoS_2 ink and the Li-exfoliated MoS_2 ink for comparison. The MoS_2 film was printed on 100 mm diameter SiO_2 wafer (Figure 3b) and further used for the fabrication of large-scale printed logic gates such as NOR and AND (Figure 3c). The patterned transistors show an overall on/off ratio of 10^6, which is much higher than the previous solution-processed MoS_2 thin-film transistors (TFTs).[105]

One general challenge of the printing technology is how to eliminate the aggregation of nanoflakes in liquids due to the large specific surface area.[104] To overcome this problem, Shao et al. reported an electrohydrodynamic-assisted method to print ultrathin 1T phase MoS_2 (Figure 3d).[106] High-purity and ultrathin MoS_2 with 1T phase (1T-MoS_2) was guaranteed by the superior fast solvent evaporation and ink solidification of the electrospray process. In this way, arrayed 1T-MoS_2 was printed on 4 in. wafer and photopaper (Figure 3e,f). The scanning electron microscope (SEM) image proves that the aggregation in solution is depressed and high-uniformity 1T-MoS_2 is successfully fabricated (Figure 3g).[106] Moreover, de Moraes et al. employed ethyl cellulose (EC) as the solvent to realize the liquid-phase exfoliation and well stabilization of h-BN nanosheets.[107] In particular, the inks with different viscosity are suitable for different printing methods and accordingly both the ink-jet printing and spin-coating technologies are employed in this study (Figure 3h). The SEM image (Figure 3i) and optical image (Figure 3j) of the printed h-BN prove that the printed h-BN exhibited a high degree of surface flatness and uniformity in a wide range. Moreover, the average thickness of h-BN is linearly tunable with the number of print passes (Figure 3k). This work successfully constructed viscosity-tunable inks for the preparation of h-BN thin films with controllable porosity, electrolyte wettability, and high ion conductivity, paving a way for fabricating high-performance electronics.[107]

Considering the natural toxicity of the ink solvent such DMF, NMP, EC, etc., printing technologies with biocompatible and nontoxic inks are also critical for the practical processing.[104] Very recently, Williams et al. reported the fabrication of all-carbon TFTs through a crystalline nanocellulose dielectric ink which is highly environmental-friendly (Figure 3l).[108] The ink is compatible with CNT and graphene, and is suitable for aerosol jet printing at room temperature (Figure 3m). The printed TFT devices on paper (Figure 3n) and the paper after ink removal (Figure 3o) demonstrate the ink is steadily reproducible.[108]

Printing technologies have significantly prompted the large-scale nanopatterning of 2D materials but remain to be improved.[92,95,104] Printing technologies are suitable for wafer scale integration and high integration density is facile to achieve in the substrate.[105] Limited by the size and precision of the nozzles, the minimal feature size is often larger than 10 μm which hinders the development of miniaturization of devices. Generally speaking, printing technologies are facile to achieve patterned preparation and avoid raw material waste.[104] However, inevitable contamination of the products after solution process will suppress the performance of FETs and hinder their application in electronics.[104,105,109] Meanwhile, the time-consuming and trivial formulation process may also limit the batch production of 2D nanopatterns.[109,110] In addition, many printing inks are toxic and expensive, which may also restrict their practical employment.[111] Thus, developing nontoxic inks and depressing their possible contamination would be essential in the following studies.

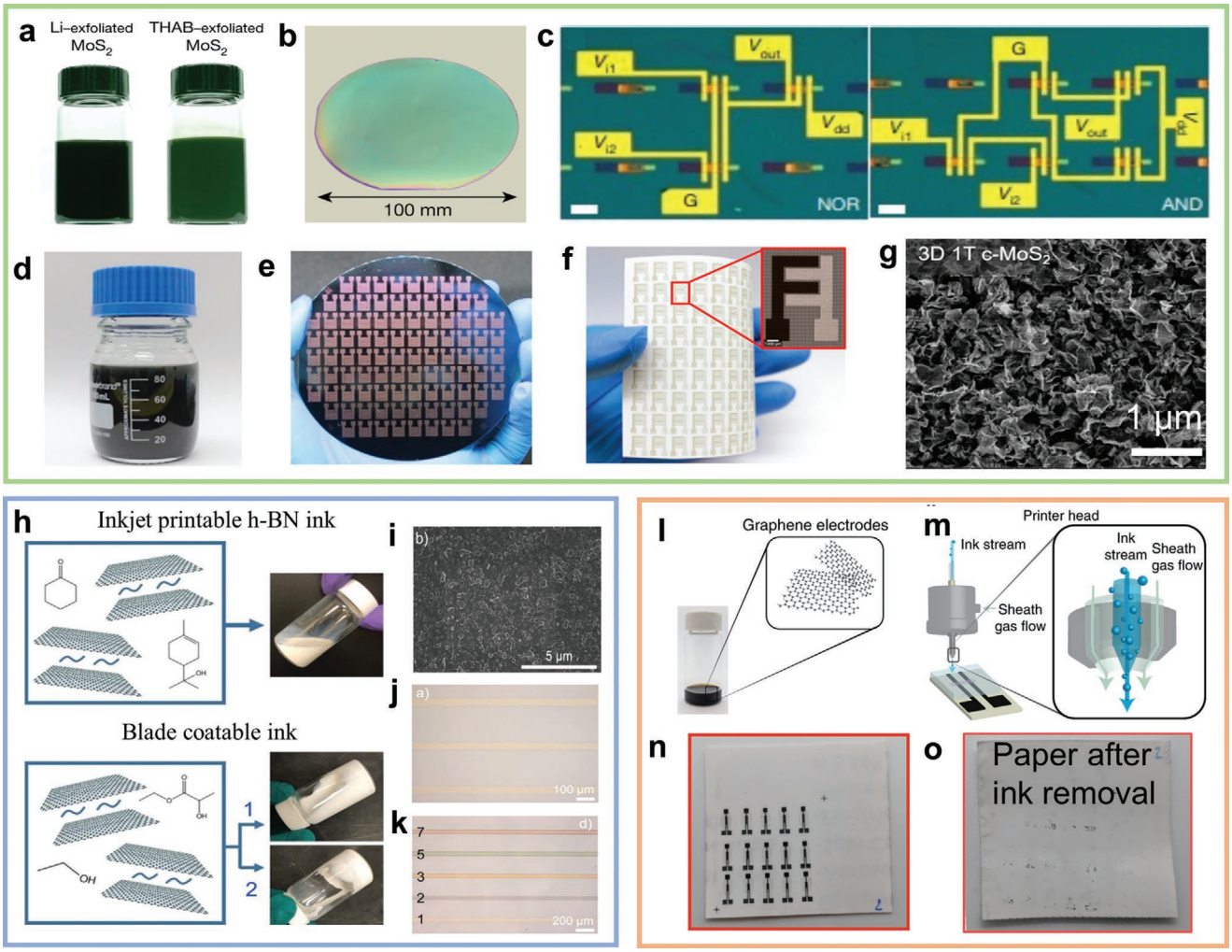

Figure 3. Printing technologies. a) Photos of Li-exfoliated and THAB-exfoliated MoS_2 ink. b) Printed MoS_2 film on 100 mm diameter SiO_2/Si wafer. c) The fabricated logic gates. a–c) Reproduced with permission.[105] Copyright 2018, Springer Nature. d) Photo of 1T phase MoS_2 ink. e,f) Printed 1T-phase MoS_2 on 4 in. SiO_2/Si wafer (e) and photopaper (f). g) SEM image of printed 1T-phase MoS_2. d–g) Reproduced with permission.[106] Copyright 2020, American Chemical Society. h) Schematic of h-BN in ethyl cellulose solution. i) SEM image of patterned h-BN. j,k) Optical image of the as-printed h-BN ribbons (j) and that with different thickness (k). h–k) Reproduced with permission.[107] Copyright 2019, Wiley-VCH. l) Exfoliated graphene ink. m) Schematic illustration of graphene aerosol jet printing technologies. n,o) Photo of printed all-carbon TFT array on paper (n) and that after ink removal (o). l–o) Reproduced with permission.[108] Copyright 2021, The Authors, published by Springer Nature.

2.1.3. Self-Assembly Technologies

Self-assembly refers to the technology by which basic structural units spontaneously form an ordered structure under the interaction based on noncovalent bonds.[112] Compared to traditional methods such as etching, deposition, etc., self-assembly effectively excludes impurities out of the system, ensuring the high quality of the obtained 2D nanopatterns.[57] Additionally, self-assembly bridges microstructures and macro-devices with low energy consumption. Self-organized graphene nanopatterns were initially reported through O_2 etching in 2013.[113] Later, self-organized TMD patterns have also been reported successively. For instance, the 1H/1T triangular pattern was successfully implemented by controlling the initial density of Se atoms on the Pt (111) surface during the self-assembly process (**Figure 4**a).[114] The scanning tunneling microscopy (STM) image (Figure 4b) shows the lateral junction structure at an atomic level. The successful evolution of such intrinsic lateral junction reveals the role of Se concentration in the phase transition between 1T and 1H $PtSe_2$. The self-organized homojunctions obtained in this study might prompt their promising applications in various electronics devices.[114]

In recent years, solution-based process, where self-assembly usually occurs, has been also exploited to fabricate 2D materials.[24,115] Lin et al. reported a two-step method to synthesize 2D nanopatterns by self-assembly of metal ions with functional group in solution.[116] The authors utilized metal ions in gelatin hydrogels as a precursor for the high-temperature synthesis of metal carbides. The gelatin served as a scaffold to impose the lamellar organization of the inorganic components with large interlayer spacings preserved after the thermal treatment. In this way, Mo and W metal ions are organized as

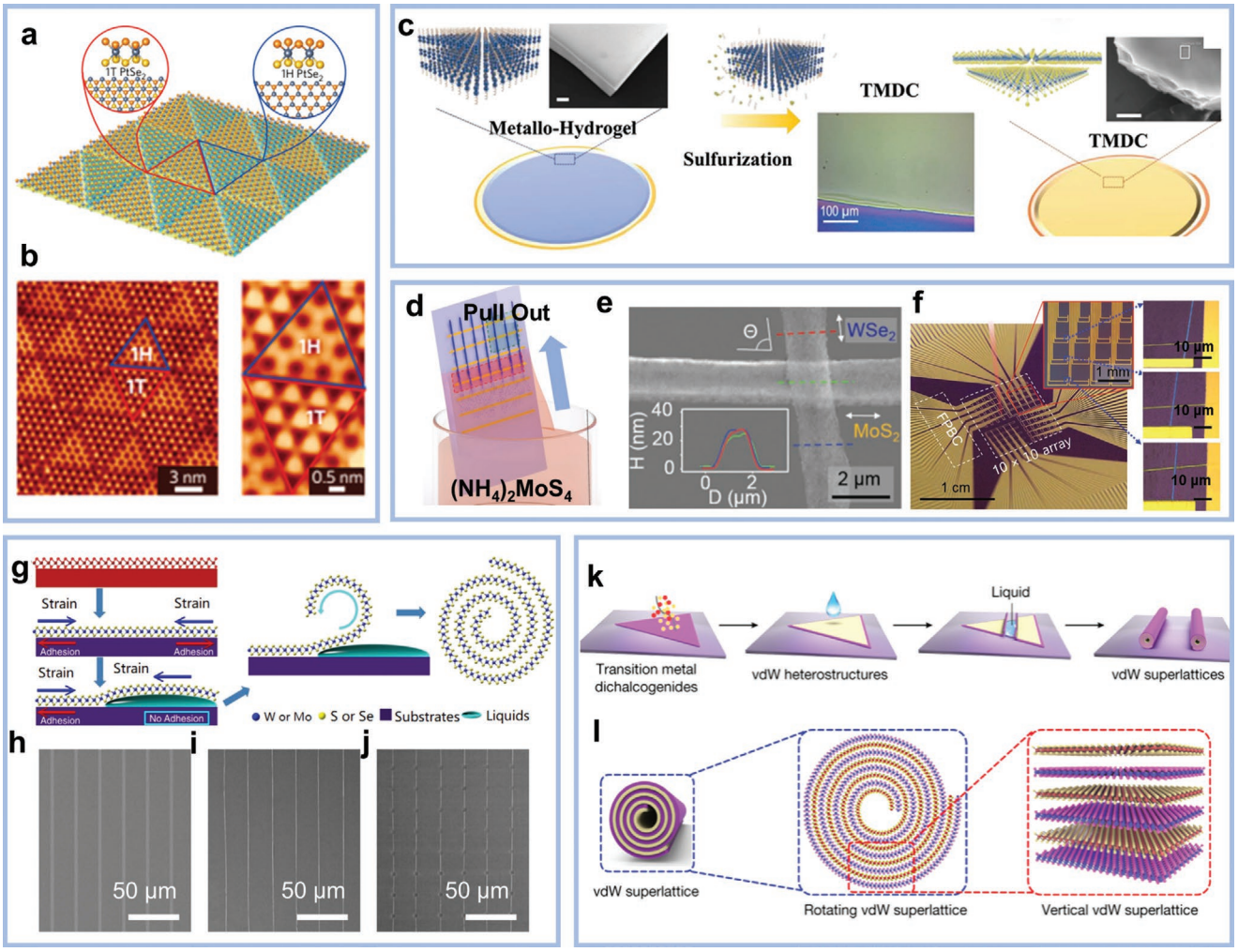

Figure 4. Self-assembly technologies. a) Schematic illustration of 1T-1H $PtSe_2$ patterns. b) STM image of 1T-1H $PtSe_2$. a,b) Reproduced with permission.[114] Copyright 2017, Springer Nature. c) Schematic illustration of the self-assembly of metal precursors for the fabrication of TMD nanopatterns. Reproduced with permission.[116] Copyright 2019, Wiley-VCH. d) Schematic for the synthesis of self-assembled WSe_2/MoS_2 heterostructure. e) SEM image of the resultant cross-aligned MoS_2/WS_2 heterostructure. f) The integrated device based on the 10×10 MoS_2/WS_2 array. d–f) Reproduced with permission.[117] Copyright 2019, Wiley-VCH. g) Schematic for the self-assembly based on the rolling technologies of 2D materials. h–j) Fabrication process of MoS_2 nanoscroll array. g–j) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[118] Copyright 2018, The Authors, published by Springer Nature. k) Schematic for the rolling process to prepare 2D superlattices. l) Structure of rolled superlattices. k,l) Reproduced with permission.[119] Copyright 2021, The Authors, published by Springer Nature.

lamellar nanostructures. Followed by the further sulfurization step, MoS_2 and WS_2 nanopatterns on SiO_2/Si substrates are obtained (Figure 4c). Such two-step indirect strategy involving the self-assembly of precursors is suitable for most 2D TMDs, yet sometimes is limited as the thickness and microstructure of the products is hard to control, and the process is often time-consuming.[116]

Moreover, the direct self-assembly of 2D materials has been used to realize the fabrication of heterojunction arrays.[24] Lee et al. developed a direct synthesis method to fabricate arrayed WSe_2/MoS_2 heterostructures through the facile solution-based directional precipitation (Figure 4d).[117] By manipulating the internal convection of the solution, WSe_2 are selectively stacked on the MoS_2 at a specific angle, so that both parallel- and cross-aligned heterostructures can be formed. Figure 4e displays the cross-aligned MoS_2/WS_2 heterostructure. The channel of MoS_2/WS_2 heterojunction could be close to 2 μm. The as-fabricated array exhibited excellent optoelectrical properties with the responsivity reaching 5.39 A W^{-1}. To further demonstrate its practical application, the authors further fabricated a photosensor device with 10×10 pixels (Figure 4f), which demonstrates promising photosensing and imaging ability. Overall, this study shows a new way to prepare 2D heterojunctions with low energy consumption and less contamination.[117]

The self-assembly strategies also provide a possibility to easily transform 2D materials into other morphologies with modulated properties.[87] Cui et al. reported a simple solution-induced assembly method that the intrinsic TMD nanoscrolls can be obtained almost nondestructively for the first time.[118] The MoS_2 was initially grown at high temperature and then cooled down to the room temperature. Due to the mismatch of thermal expansion between MoS_2 and the substrate, inherent

strain was introduced to the flake. Ethanal solution was then spread to the surface of the MoS_2 flake and embedded between the MoS_2 flake and substrates. The MoS_2 flake was released from the substrates to be freestanding. Under inherent strain, the freestanding part of the flake curved out of the plane and continues to roll up in solution to form nanoscrolls. The whole process is illustrated in Figure 4g. By utilizing this method, the authors subsequently fabricated MoS_2 nanoscroll arrays. First, MoS_2 polycrystalline film is synthesized and then etched to form parallel ribbons with defined width and direction (Figure 4h). Second, the authors rolled nanoribbons up to obtain nanoscrolls array (Figure 4i). Last, long nanoscrolls are etched to periodic short nanoscrolls (Figure 4j). Based on its unique spiral structure, the entire nanoscrolls can participate in the transport of carriers. Compared with the single-layer TMDs, the mobility of the FET based on the nanoscrolls is 30 times higher. The unique self-encapsulation structure enables TMD nanoscrolls to exhibit higher optical and electrical stability.[118]

Besides monolayer TMDs, such self-assembly method can also be applied for vdW heterojunctions (Figure 4k).[119] Recently, Zhao et al. reported a facile approach to construct highly ordered SnS_2/WSe_2 vdW superlattices by rolling up SnS_2/WSe_2 vdW heterostructures (Figure 4l).[119] The authors proved that the capillary force could drive a spontaneous delamination and rolling-up process to produce vdW heterostructure roll-ups containing high-order 2D/2D vdW superlattices without going through multiple transfer and trivial restacking. This method driven by the capillary force helps to solve the contamination during the transfer process to fabricate heterojunction. Such diverse high-order vdW superlattices are found to exhibit designable band offset and chirality, which provides a platform to study the rational tuning of the carrier confinement or carrier separation.[119]

Overall, the self-assembly approaches widely broaden the routes to fabricate nanopatterns of 2D materials with high efficiency and low cost, despite it is currently not yet universal for all material systems.[57] The process of self-assembly excludes many irrelevant materials so as to ensure the purity of patterned 2D materials. The whole process of self-assembly requires less energy supply, which prominently decreases the energy cost. At the same time, the process of self-assembly is always intensively affected by the disturbance of the environment, which may not benefit the batch production.

2.2. Top-Down Methods

Top-down methods involve the presynthesis of large-scale and uniform 2D materials, and then applying advanced nanofabrication techniques to obtain specific patterns.[58] The nanofabrication cuts and crops 2D materials to the desired geometries like a scissor. However, due to the precision limit of current nanofabrication instruments at the atomic scale, inevitable edge defects and morphology inconsistency caused by the top-down methods might degrade the device performance.[120] According to whether photolithography is applied, we divide the top-down methods into two categories: 1) lithographic etching technologies, 2) direct writing technologies.[58]

2.2.1. Lithographic Etching Technologies

As a typical top-down method to obtain 2D nanopatterns, the lithographic etching technologies usually involve the preformation of nanopatterns with the specifically designed masks, followed by utilizing plasma or solutions to corrode the 2D materials under the protection of the patterned photoresists.[121,122] In a typical photolithographic etching process, the photoresist is dispensed from the viscous polymer solution to the center of substrates through spin coating. To remove solution and eliminate the strain built-in after spin coating, the baking process is then employed. After aligning the mask on the substrates, exposure with UV light is successively implemented. The development process is then applied to remove the photoresist on the exposure region. Consequently, the specific pattern is exposed to the air and photoresist covers the part of target patterns. Followed by etching process and lift-off, the patterned 2D materials were successfully fabricated.[123,124]

According to the etching mediums, the etching processes are generally divided into dry and wet etching.[57] The dry etching refers to chemical reactions activated by plasma or physical removal using high-energy ion beam bombardment without solution participating (Figure 1d). The low-pressure gas discharges to form plasma, which is the basis of dry etching. Reactive ion etching (RIE) is a mature commercial dry etching method to obtain the specific microstructures in silicon-based IC manufacturing.[4,125,126] In an RIE chamber, corrosive gas, such as CHF_3, CF_4, and SF_6, is ionized via high voltage. Ions, electrons, and free radicals (free-state atoms, molecules, or clusters of atoms) produced by inelastic collisions, also known as plasma, have strong chemical activity and can react with atoms on the surface of the etched sample and form volatile substances to corrode the surface of the sample.[127,128] Compared to the traditional semiconductors, 2D materials usually have an atomic thickness, which can be etched more easily by the high-energy plasma.[129] Thus, by precisely controlling etching parameters, it is possible to fabricate 2D nanopatterns with an arbitrary thickness.

The etching of bulk MoS_2 by SF_6 to achieve the controlled fabrication of large-area patterned arrays was initially reported in 2013.[40] Li et al. further employed RIE to fabricate MoS_2 nanoribbon with different width.[130] In this work, the authors found that the inevitable photoresist residues and defects induced by RIE process might cause a decrease in thermal conductivity. Meanwhile, increased absorption and scattering efficiency can be observed with the decrease of ribbon width, and accordingly, the optoelectronic performance of the nanoribbon products can be effectively modulated.[130] Arrayed 2D devices fabricated by RIE are also found to exhibit splendid electronic performance. Conti et al. utilized SF_6 to etch MoS_2 on the sapphire to obtain a specific pattern of MoS_2 (**Figure 5**a).[131] The on/off ratio and mobility of as-fabricated MoS_2 array device (Figure 5b) reach 8×10^3 and 5.5 $cm^2 V^{-1} s^{-1}$, respectively.

In addition, the RIE process ensures a good performance consistency of arrayed nanopatterns.[132] Recently, Li et al. successfully employed RIE to fabricate MoS_2 FET array (Figure 5c).[133] The electron mobility and subthreshold swing (SS) keep the same level among different devices (Figure 5d). The FET arrays exhibit excellent performance consistency,

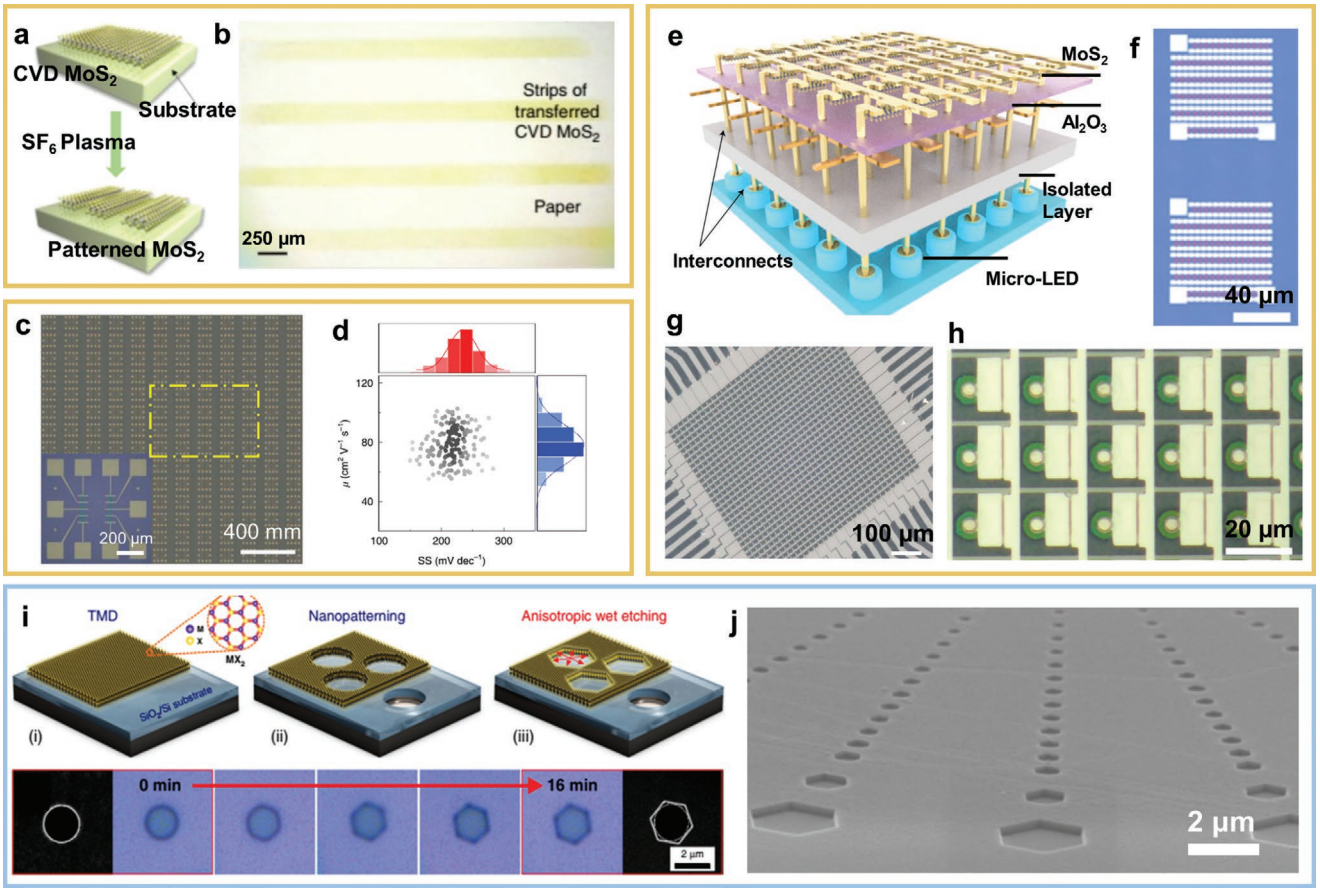

Figure 5. Lithographic etching technologies. a) Schematic illustration of RIE etching process. b) Optical image of MoS_2 strips after etching. a,b) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[131] Copyright 2020, The Authors, published by Springer Nature. c) Schematic for the MoS_2 FET array and d) the corresponding SS and carrier mobility distribution. c,d) Reproduced with permission.[133] Copyright 2021, The Authors, published by Springer Nature. e) Schematic of TFT-micro-LED integrated device made by the RIE fabrication of MoS_2. f) Optical image of MoS_2 TFTs fabricated by RIE. g,h) Optical images of micro-LED arrays. e–h) Reproduced with permission.[134] Copyright 2021, The Authors, published by Nature Publishing Group. i) Schematic illustration of the wet anisotropy etching process for TMDs and its morphology evolution. j) SEM image of the etched WS_2. i,j) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[135] Copyright 2020, The Authors, published by Springer Nature.

further indicating that RIE is widely compatible with 2D materials.[133] Almost at the same time, the same group fabricated MoS_2 TFTs by CF_4 RIE etching (Figure 5e,f).[134] In this work, excellent high-resolution displays were successfully realized by integration of MoS_2 TFT and nitride micro-light-emitting diodes (LEDs; Figure 5g,h). This further implied that RIE will significantly favor the actual application of 2D materials.[134]

Wet etching is another universal method to manufacture silicon-based microelectronics (Figure 1e). Despite the successful applications of various wet etching techniques in silicon materials, their development in 2D materials is relatively slow due to the limitations of selecting widely acceptable etching solvents. With this regard, Munkhbat et al. reported a facile and controllable method to realize the anisotropic etch of TMDs with atomic precision.[135] After EBL and RIE, circle holes formed on the surface (Figure 5i). When TMDs with holes were put into the solution, anisotropic etching process was conducted, and arrayed TMD hexogen holes were accordingly fabricated after the etching. SEM image shows the etched holes are in perfect consistency for both morphology and size (Figure 5j).[135]

As a summary, the etching process is particularly suitable for large-area processing, making it of great promise for batch production.[132,136] The minimal feature size is close to sub-10 nm. In addition, etching technologies are compatible with modern semiconductor integration process, which possibly makes 2D materials easy to be integrated on silicon-based substrates.[137–139] Etching technologies are suitable for batch production which has been widely employed in the silicon-based industry. Still, the photoresist residues will hinder the application of 2D materials. Adding buffer layer between 2D materials and photoresist may remove the photoresist residues.[140] Also, resist-free lithography is recently proved. Resist-free lithography could keep the surface clean and flat without resist residues.[31] Besides, uncontrollable edge defects caused by etching process is harmful for industrial production. Revealing the mechanism of etching process and controlling the etching rate will depress the edge defects. To realize this, new gas RIE systems suitable for 2D materials need further exploring. Also, anisotropic etching technologies are not well developed for 2D materials which may bring etching technologies to atomic level.[135]

2.2.2. Direct-Writing Technologies

To exclude the influence of photoresist residues on the surface of 2D materials, direct writing technologies are recently explored for 2D nanopattern fabrication.[141–143] Probes and lasers are two essential direct writing tools (Figure 1f,g). For instance, scanning probe lithography (SPL) has been recently used to directly pattern single-layer TMDs without using the sacrificial resists.[144–146] Tip-induced oxidation, thermal decomposition, and mechanical scratching are standard SPL techniques for 2D nanopattern fabrication. Zhao et al. put a negatively biased tip close to the TMDs surface with an atomic force microscope (AFM; **Figure 6**a).[147] By establishing a water bridge between the tip and the TMD surface, controlled oxidation can be achieved at sub-100 nm resolution. The oxidized flakes are then immersed in water to remove oxides selectively, thereby forming a controllable pattern. In addition, by changing the oxidation time, the thickness-tunable pattern of the multilayer TMDs is successfully fabricated. By controlling the tip bias, amplitude setpoint, and humidity, patterned 2D materials with controllable size are successfully fabricated (Figure 6b). Such photoresist-free process results in edge exposure, which might overcome the obstacles in traditional resist-based lithography and dry etching, where polymer byproduct layers are usually formed at the edges.[147]

Besides tip-induced oxidation, thermal decomposition by tip has also been applied to fabricate 2D nanopatterns.[148] Liu et al. proposed a nanocutting technique for direct cutting of 2D materials combining force and heat to break the chemical bond of 2D materials.[45] In this work, local thermomechanical separation of the chemical bonds between 2D materials is achieved through heated nanotips under ambient pressure and temperature (Figure 6c). Before patterning process, the TMDs are transferred onto a polymer layer on SiO_2/Si substrate. With the temperature of the tip reaching 150 °C, the polymer underneath the 2D materials sublimates quickly and forms into small volatile molecules. The sublimated region provides enough space for tip to press 2D materials deep enough to break the chemical bonds, forming the specific 2D nanopatterns. The AFM image of patterned $MoTe_2$ (Figure 6d) and the depth variation along

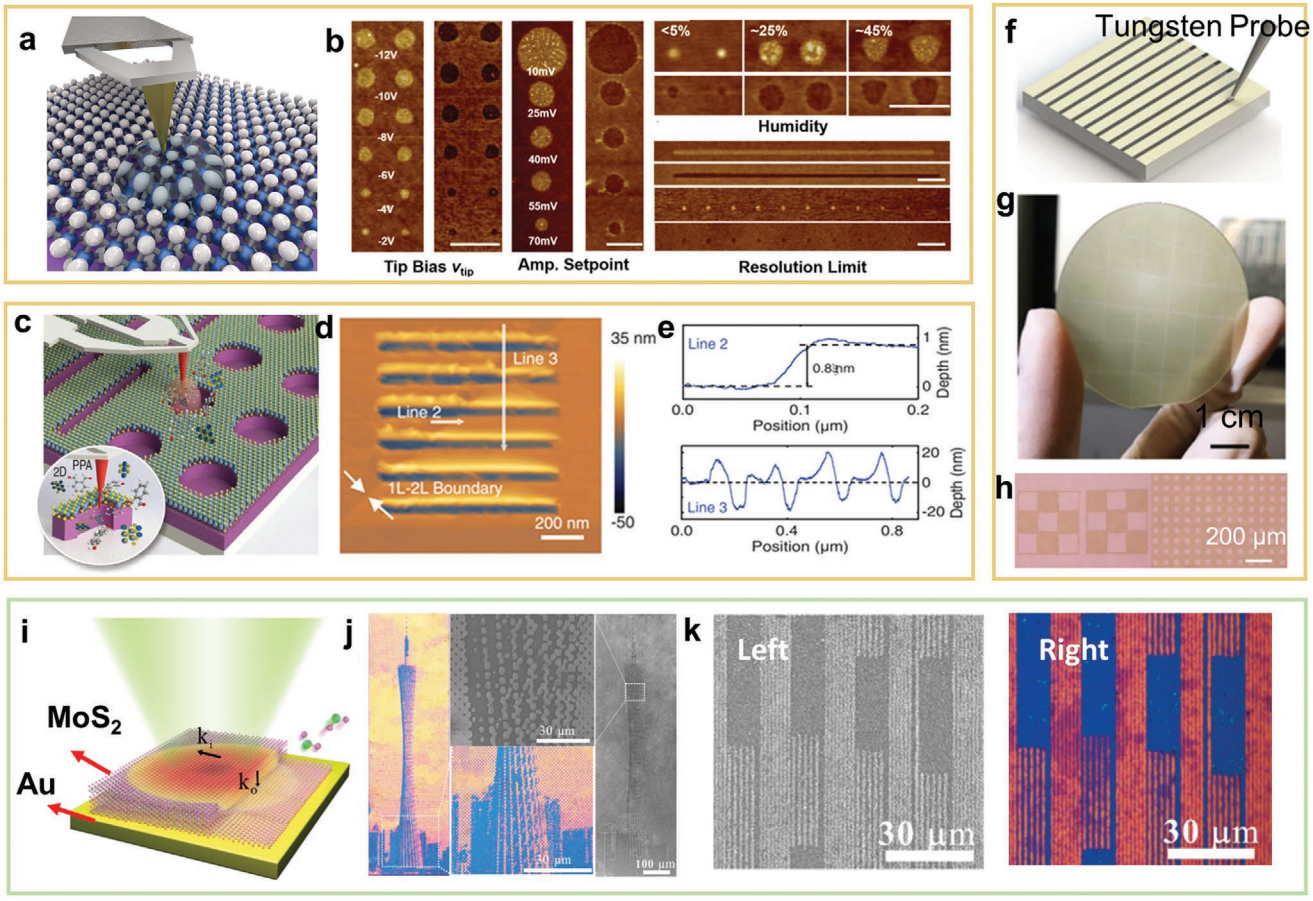

Figure 6. Direct writing technologies. a) Schematic of tip-induced oxidation of 2D materials. b) AFM demonstration of patterned MoS_2 under different technical conditions. a,b) Reproduced with permission.[147] Copyright 2019, Wiley-VCH. c) Schematic for the thermal nanocutting technologies. d) AFM image of patterned MoS_2 and e) the corresponding depth variation with position. c–e) Reproduced with permission.[45] Copyright 2020, The Authors, published by Wiley-VCH. f) Schematic of the scratch lithography. g,h) The resultant patterned MoS_2 on sapphire. f–h) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[46] Copyright 2020, The Authors, published by IOP Publishing Ltd. i) Schematic illustration of laser exfoliation for MoS_2. j,k) The obtained nanoplane color printing image (j) and binocular stereo image (k). i–k) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[154] Copyright 2020, The Authors, published by Springer Nature.

the graved line (Figure 6e) demonstrates a high-resolution of 20 nm for the obtained single-layer $MoTe_2$. Besides, the authors show that other TMDs such as MoS_2 and $MoSe_2$ could also be processed by this method.[45]

In addition, mechanical scratching also has been developed for preparing 2D nanopatterns.[149] Recently, Wei et al. demonstrate a scratching lithography method to prepare patterned 2D materials.[46] Like the traditional engraving technology, this method uses an electric displacement system built in the glove box to mechanically scratch the metal tungsten tip on the surface of the 2D materials to achieve direct writing (Figure 6f). It is worth noting that this method is suitable for the patterned processing of wafer-level 2D materials (Figure 6g). In this way, various patterned MoS_2 on sapphire wafer was fabricated in this study (Figure 6h). Its accuracy can reach about 1 μm, which is close to the accuracy of UV lithography as stated by the authors.[46]

Laser processing has been realized as another critical direct writing technology for the fabrication of 2D nanopatterns (Figure 1g).[150] Zheng et al. reported an all-optical lithographic technique, namely, optothermo-plasmonic nanolithography, which was developed to achieve high-throughput, versatile, and maskless patterning of different atomic layers.[151] Before this work, femtosecond laser processing for 2D materials had been realized but high optical power hindered its development.[152,153] By using thermal oxidation and sublimation at highly localized thermal plasma hot spots, high-resolution patterning of graphene and MoS_2 monolayers is successfully fabricated with low optical power (6.4 mW μm^{-2}).[150]

Moreover, the intrinsic properties of 2D materials can also be used to improve the precision of laser processing. By utilizing the interlayer vdW interactions and anisotropic thermal conductivity of 2D materials, Li et al. demonstrated ultra-sensitive light field manipulation in resonance spectra by nanometrically maneuvering the thickness of MoS_2 layers through a laser exfoliation technique (Figure 6i).[154] For vdW 2D materials, interactions between layers are weak, and accordingly heat dissipation dominantly propagates along the in-plane direction rather than out-plane direction. The giant temperature gradient between the upper layer and the beneath layer makes the upper layer decompose. Under this mechanism, precisely controlling the reliable thickness of 2D vdW materials is facile to achieve, resulting in the successful fabrication of high-fidelity color image (Figure 6j). Moreover, the further amplitude-modulated diffraction component for binocular stereo images (Figure 6k) can be realized in a simple and nonlithographic way.[154]

In directing-writing technologies, the essential use of masks and photoresist could be possibly avoided, making the customized patterns easy to fabricate and the overall process more environmental-friendly.[144,146] The minimal feature size of the 2D materials could approach 500 nm which is close to the UV lithography technologies. Moreover, the 2D nanopatterns are possible to fabricate within one step by using the direct writing technologies, which simplifies the whole process and ensures the clean surface of 2D materials.[150] However, direct writing usually requires a relatively long time to achieve high resolution of the products at atomic and molecular scale, resulting in the higher cost and more energy consumption as compared to the photolithographic techniques.[144] Consequently, the wafer scale patterning tasks are difficult to be completed by direct writing technologies.

3. Nanopatterning for 2D Integrated Devices

The performance of silicon-based chips has been found to be more and more difficult to make significant breakthrough in recent years.[6,155] Nanopatterning technologies for 2D materials enable it to be applied in the next-generation electronic and optoelectronic devices. On the one hand, nanopatterning technologies ensure the device performance consistence and depress the variation between different devices, which is fundamental for ICs. On the other hand, nanopatterning technologies enable 2D materials to be integrated in various device structures in large areas to achieve different functions. For example, single FET device could not execute computing tasks while integrated FET devices could be designed with proper feature size to form logic gates. However, the unmatured patterning technologies make many scientific researches of 2D materials stay on the single device level. With the continuous development of nanopatterning technologies, not only various logic gates based on 2D materials have been realized, but also novel device structures such as memristors and artificial synapses have been put forward and suggested to be promising.[156] The key metrics including feature size, integration scale, and corresponding applications are summarized in **Table 1**. In this section, we summarize the recent development of integrated 2D electronic and optoelectronic devices, emphasizing the critical function of nanopatterning for the device construction.

3.1. Integrated Logic Circuits

FETs based on 2D materials have well-developed in last decade.[4,156] Very large-scale integration circuit (VLSI) is based on FETs which are combined to achieve basic functions of logic gates such as INVERTOR, NAND, NOR, and AND.[13,14] Nanopatterning technologies closely relate to the performance of the integrated devices. For example, higher integration density benefits the computing ability. Although the microprocessor is successfully fabricated in millimeter scale.[157] The integration density is still not high enough to meet the demand of miniaturization and wafer-scale fabrication. To improve the computing ability, the lateral channel length of the 2D materials has been close to the sub-100 nm and the side-wall vertical channel length has been put forward.[47]

Recently, wafer-scale 2D nanopatterns for ICs have been realized via various patterning technologies mentioned above. Dathbun et al. successfully prepared large-scale multi-layer ReS_2 on SiO_2/Si substrates, which was further fabricated into logic gates through RIE (**Figure 7**a). The patterned graphene was then transferred to serve as source, drain, and gates, resulting in a maximum electron mobility of 0.9 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio exceeding 10^4 (Figure 7b).[158] In this study, the prepatterned 2D materials are easy to fabricate FET devices, which simplifies the whole integrated process including spin-coating and lithography. The nanopatterning technologies could also omit the transfer process. Yeh et al. recently conducted the

Table 1. Key metrics of nanopatterning methods and corresponding application.

Materials	Device structure	Nanopatterning methods	Feature size length	Feature size width	Integration scale	Ref.
MoS_2	Logic gates	RIE	3 μm	3 μm	54 640 FETs	[9]
$MoTe_2$	Logic gates	Induced growth	400 nm	100 nm	1644 FETs	[197]
MoS_2	FET	Printing technology	100 μm	50 μm	Wafer scale	[105]
Graphene electrodes	FET	Printing technology	600 μm	200 μm	320 FETs	[50]
MoS_2	ICs	RIE	20 μm	20 μm	1296 FETs	[48]
MoS_2	FET	RIE	500 μm	40 μm	26 FETs	[131]
Graphene	FET	Etched by oxygen plasma	1 μm	500 nm	192 FETs	[198]
ReS_2	Logic gates	RIE	2 mm	250 μm	10 × 5 FETs	[158]
WS_2/WSe_2 channel	Logic gates	RIE (CF_4/O_2)	500 μm	100 μm	10 × 5 FETs	[49]
MoS_2	FETs	Etched by oxygen plasma	5 μm	30 nm	Wafer scale	[47]
$PdTe_2$ electrodes	FETs	Induced growth	5 μm	5 μm	Wafer scale	[199]
MoS_2	Microprocessor	Etched by Ar/O_2 Plasma	15 μm	5 μm	Millimeter-level Scale	[157]
MoS_2	FGFETs	Etched by oxygen plasma	10 μm	2 μm	40 FGFETs	[162]
MoS_2	Transistors	DRIE (CHF_3/O_2)	5 μm	2 μm	12 FETs	[164]
PO_x/BP	Memristor crossbar	EBL	100 nm	100 nm	10 × 10	[200]
h-BN/graphene/h-BN	Memristor crossbar	RIE	500 nm	500 nm	12 × 12	[44]
Au/Ag/h-BN/Ag/Ti	Memristor crossbar	Lithography	750 nm	750 nm	10 × 10	[43]
$Al/MoS_2–MoO_x/Al$	Memristor crossbar	RIE(CF_4)	30 μm	30 μm	Wafer scale 19 446 unit cells	[201]
MoS_2 channel	Memristor crossbar	RIE	900 nm	700 nm	9 × 10	[165]
MoS_2 channel	Memristor crossbar	RIE (CHF_3/O_2)	20 μm	400 nm	10 × 10	[202]
$PtTe_x$	Photodetector array	Induced growth	100 μm	100 μm	10 × 10	[180]
MoS_2	Photodetector array	RIE	50 μm	50 μm	32 × 32	[181]
WSe_2	Photodiodes	EBL	10 μm	1.5 μm	3 × 3	[183]

epitaxy growth of WS_2 and WSe_2 where graphene serves as a template to reduce the contact resistance via lateral contact.[49] Prior to the epitaxy growth, the photolithography and RIE (CF_4/O_2) were applied to fabricate the graphene nanopatterns. The etched part of graphene was defined as the channel region for the epitaxy growth of WS_2 and WSe_2 (Figure 7c). In this way, site-selective synthesis of complementary n- and p-channels semiconductor was achieved, resulting in a transparent contact with a nearly ideal pinning factor of 0.95 for the n-channel WS_2 and 0.92 for the p-channel WSe_2 (Figure 7d). In this study, the induced growth for fabricating p-n heterojunctions did not require trivial transfer process in which 2D materials are easily broken. Additionally, the as-grown graphene–TMD interface exhibits an atomic level transition with low contact resistance, which significantly improves the electrical performance of the device.[49]

To further simplify the trivial integration flow, Lim et al. employed the ink-jet printing technology to fabricate all the electronic components, including the indium-gallium-zinc-oxide semiconductor, indium-tin-oxide electrodes, and the ion-gel gate dielectric, and successfully constructed vertical SB transistors on a 4 in. SiO_2/Si wafer (Figure 7e).[50] In the recent reports, printing technologies for electrodes significantly depress the formation of the defects on the metal–TMD interfaces.[93] Such all-printing technology developed in this study paves a way to construct large-scale logic gate devices with a time-saving and low-cost manner, yet might be limited by the polycrystalline structure of the products when ultrahigh device performances are required.[50]

Most recently, nanopatterning technologies makes sub-1 nm channel possible.[47] Wu et al. utilized the as-grown MoS_2 film to fabricate the 0.34 nm gate length side-wall transistor (Figure 7f,g). The as-grown MoS_2 film was patterned by oxygen plasma etching and transferred on the 2 in. wafer (Figure 7h). The channel length is currently the shortest compared to all the other FET devices (Figure 7f).[47] In addition, artificial intelligence emerges to optimize the whole process of chip manufacture industry.[159] Recently, Chen et al. applied the machine learning algorithm to wafer-scale device manufacturing (Figure 7j).[48] The key parameters of the patterning process are optimized. Based on the large experimental data sample set that has been accumulated, the authors successfully identified the device process characteristics with excellent device indicators. In this work, 4-bit adder (Figure 7k) and other functional circuit components are fabricated, greatly promoting the application of 2D materials in ICs. Besides, the intelligent device architectures can potentially be integrated into 3D circuits with dense logic and memory layers for future low-power and processing-in-memory computing applications.[48]

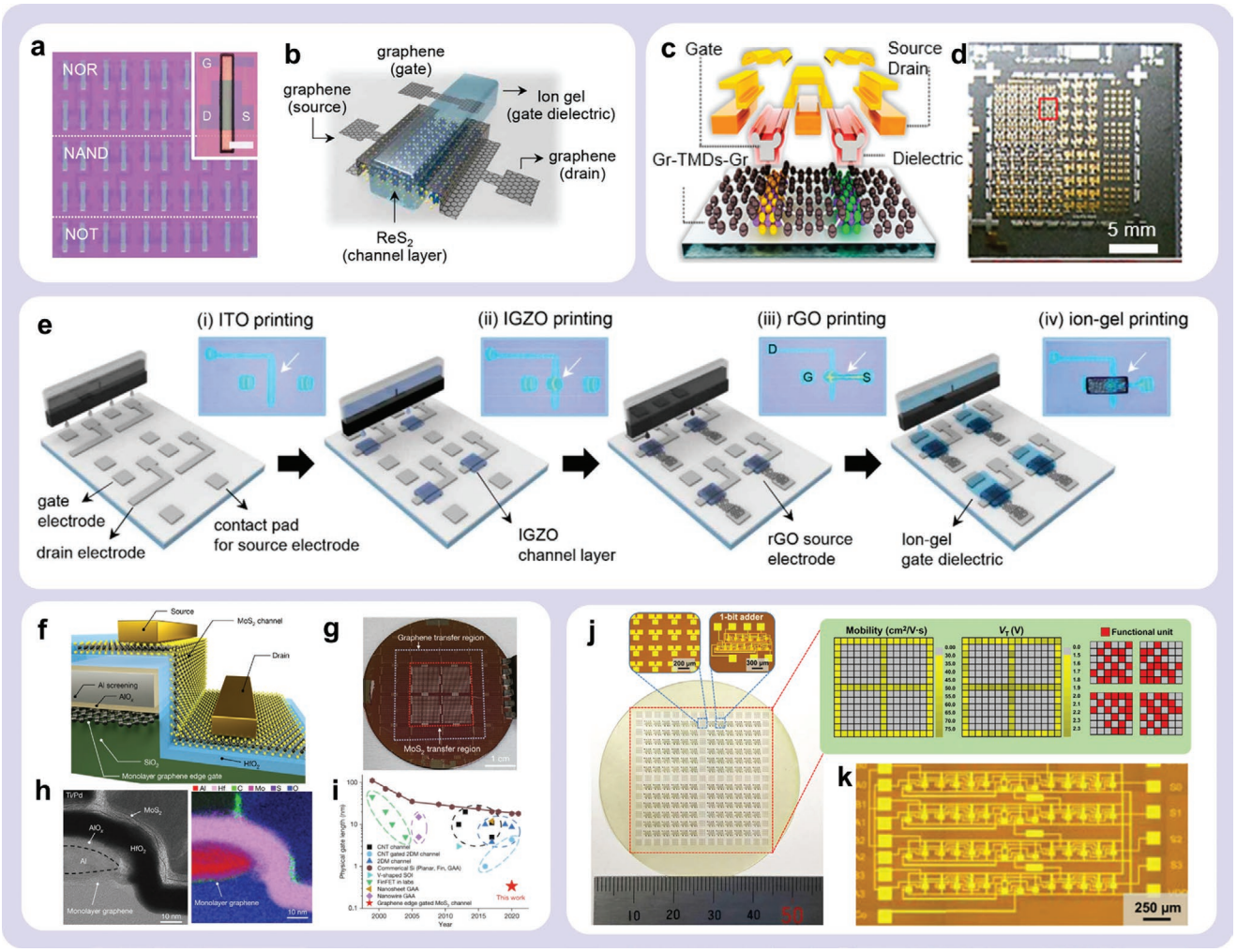

Figure 7. Integrated logic circuits. a) ReS_2 nanoribbons arrays obtained by RIE and b) the corresponding device structure. a,b) Reproduced with permission.[158] Copyright 2017, American Chemical Society. c) Schematic of the Gr/WS_2/Gr device structure. d) Optical image of the resultant 2D ICs array. c,d) Reproduced with permission.[49] Copyright 2020, American Chemical Society. e) Schematic illustration of device fabrication process based on the printing technology. Reproduced with permission.[50] Copyright 2019, American Chemical Society. f) Schematic illustration of sub-1 nm gate channel device structure. g) Optical image of FET arrays on 2 in. wafer. h) SEM image of sub-1 nm gate channel and corresponding EDX mapping. i) The channel length based on different materials. f–i) Reproduced with permission.[47] Copyright 2022, The Authors, published by Springer Nature. j,k) RIE-based fabrication of FET array for 1-bit adder and 4-bit adder. j,k) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[48] Copyright 2021, The Authors, published by Springer Nature.

3.2. Memory Devices

Another critical and unique merit of 2D-based integrated devices is their potential application in novel memory systems, which have been recently significantly prompted by the rapid development of 2D nanopatterning technologies.[22] As we know, nowadays conventional computing systems based on the von Neumann architecture have been unable to bear the heavy task of big data processing because of their separated data storage and processing units.[13,160] This causes significant time delay and a large amount of energy loss in the process of data transmission.[13,14,161] As a typical non-von Neumann architecture, 2D memory computing has attracted great attention. It fundamentally breaks the von Neumann architecture and realizes the fusion of processing unit and storage unit. To achieve novel device structure fabrication, nanopatterning technologies are indispensable. Also, during the patterning process, maintaining the surface clean is important. The flatness and uniformity of the surface significantly affect the memory performance. When defects exist in the surface, the electrons are easily trapped so as to suppress the speed of erase and write. Developed nanopatterning technologies which could keep the surface clean will greatly promote the application of memory devices.

Kis et al. fabricated the floating-gate field-effect transistors (FGFETs) using large-area MoS_2 as an active channel material (**Figure 8**a).[162] The as-grown MoS_2 was patterned by the RIE after EBL process. The FGFETs were then successfully fabricated with big memory window, excellent retention, durability, and multilevel storage capability (Figure 8b). To further achieve in-memory computing, the FGFETs served as building blocks for 12 mm × 12 mm die with logic-in-memory cell arrays

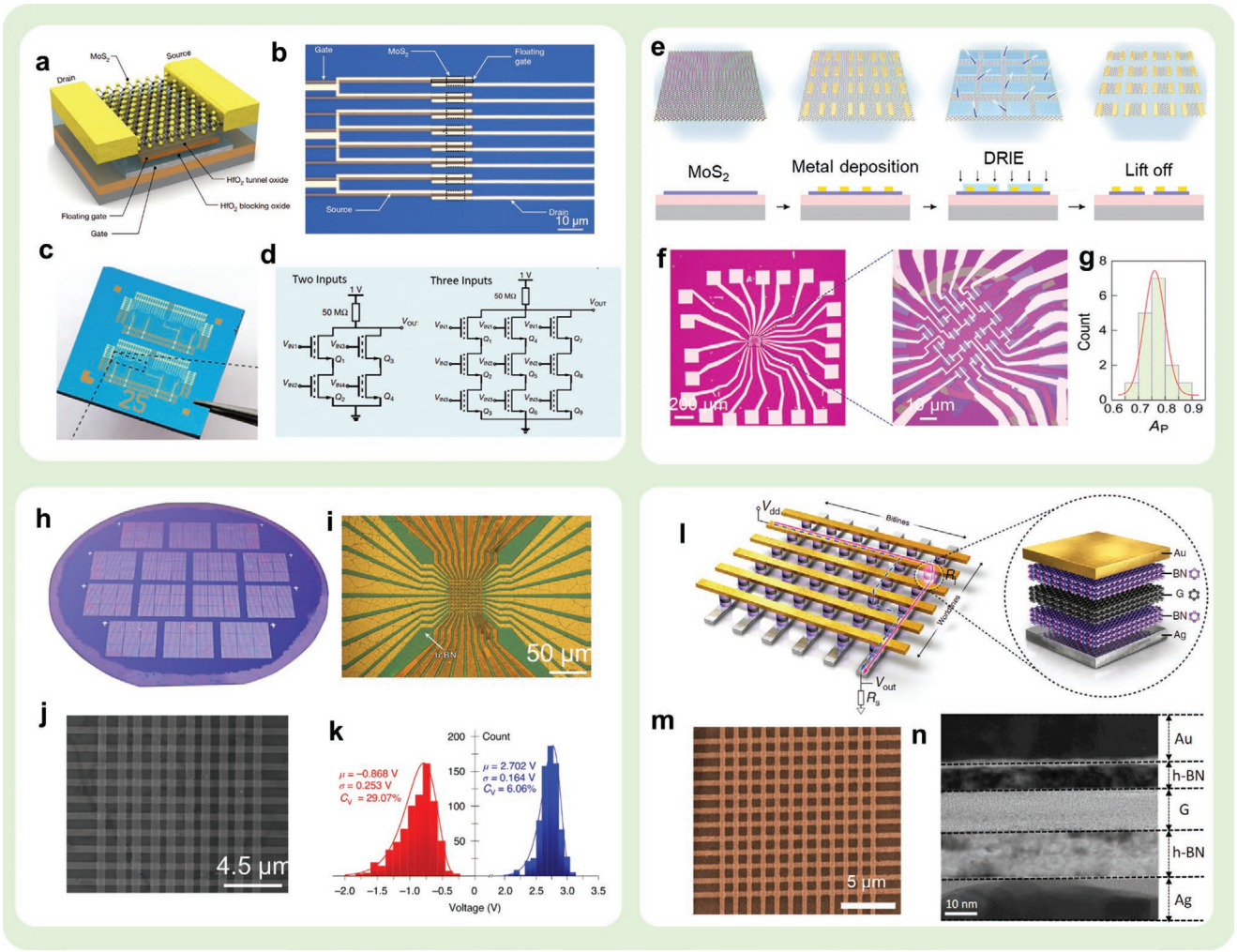

Figure 8. Memory devices. a,b) Schematic of a floating-gate memory device based on monolayer MoS_2 ande optical image of device arrays. c,d) Logic-in-memory cell arrays made by EBL. a–d) Reproduced with permission.[162] Copyright 2020, The Authors, published by Springer Nature. e) Schematic illustration for DRIE fabrication process of the sr-SiN_x synaptic array using MoS_2 as the channel. f) Optical image of sr-SiN_x synaptic array and g) the corresponding histogram of its memory performance to demonstrate the device variability. e–g) Reproduced with permission.[164] Copyright 2021, American Chemical Society. h,i) Optical images of memristor crossbar arrays based on h-BN. j) SEM image of the memristor crossbar arrays. k) Cumulative distribution of device set voltages and reset voltages of 48 devices to demonstrate the device variability. h–k) Reproduced with permission.[43] Copyright 2020, The Authors, published by Springer Nature. l) Schematic of the crossbar memory array architecture based on van der Waals heterostructure of h-BN and graphene. m,n) SEM images of 12 × 12 memristor crossbar corresponding cross-sectional TEM image of a device. l–n) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[44] Copyright 2019, The Authors, published by Springer Nature.

(Figure 8c,d). To achieve this, it is critical to precisely control the position of 2D materials and ensure the performance consistence of devices during MoS_2 pattern process.

In addition to FGFETs, devices with common FET structures constructed from 2D materials can also be used as excellent memory devices.[163] Xiang et al. reported a 2D TMD-based FET memory array fabricated on a commercial silicon-rich silicon nitride (sr-SiN_x) substrate.[164] The array was fabricated through deep RIE (DRIE) process by using the CHF_3/O_2 (Figure 8e). The array exhibits excellent uniformity, a high analog on/off ratio, and linear conductance (Figure 8f). To evaluate the variation between different devices, the long-term potential linearity (A_p) of different devices is counted and Gaussian fitting is employed, where variability (σ/μ) is determined as 1.5% (Figure 8g).[164]

Another widely studied memory device is the memristor, which is usually fabricated in the form of crossbar array.[165,166] The amount of crossbar arrays determines the computing ability. To enhance the computing ability and meet the demand of chip miniaturization, the high density of memristive crossbar arrays is significant. As a result, it is important to develop nanopatterning technologies which are suitable for large-scale fabrication and capable of high precision. Chen et al. proposed that the 2D h-BN can be used as a resistance material for high-density memristive arrays, and a device can be used for artificial neural networks for image recognition.[43] The 10 × 10 memristor crossbar arrays are integrated on the 4 in. wafer with high density (Figure 8i,k). The SEM image demonstrated the uniformity of the crossbar arrays with width of 150 nm. This

crossbar arrays exhibited excellent device variability (as low as 5.74%).[43] Also, Sun et al. fabricated a 12 × 12 memristive crossbar array based on h-BN and graphene (Figure 8l,m).[44] The bottom electrodes (Ag) were prepared by UV photolithography and thermal deposition. The graphene/h-BN heterostructures are transferred on the bottom electrodes and RIE process was carried out to remove the unnecessary part. The top electrodes (Au) were prepared right above the heterostructures (Figure 8n). In addition, compared with the common memristors, this self-selective memory greatly reduces the sneaking current over a large voltage window, opening the door to develop energy-efficient memory by integrating large-scale crossbar array.[44]

3.3. Optoelectronic Devices

2D materials possess various electronic structures and highly adjustable band gaps, which greatly enrich their optical response in a wider range of wavelengths, resulting in different photoelectric properties from traditional 3D bulk materials.[167–169] Such excellent tunable physical properties make them suitable for various functional optoelectronic devices.[170–172] In addition, since the surface of the 2D material has no dangling bonds, it is naturally ideal for integration. Optoelectronic devices based on individual 2D nanoflakes have been demonstrated to exhibit excellent performance, but still limited for practical integration applications because of their individual and separate device structure.[173–175] Recently, miniaturization of optoelectronics devices has emerged which requires the high integration density of devices. However, with the decrease of the feature size, the edges and defects on the 2D materials will inevitably increase, prominently tuning the band structure. [176–178] For example, the PL peak (659 nm) of 1D MoS_2 nanobelts exhibited a blueshift caused by edge-boundary exciton-quenching.[52] As a result, nanopatterning technologies with high precision and less destruction are critical for integrated optoelectronics.

Based on in situ transformation and RIE process, various integrated photodetector arrays based on 2D materials have been pioneeringly reported.[54,172,179] Very recently, Li et al. reported an optical noncontact controlling system (ONCS) based on $PtTe_x$/Si photodetector arrays.[180] The photodetector arrays are fabricated through lithography-assisted in situ transformation. The platinum was deposited on silicon substrates by magnetron sputtering and then transformed into $PtTe_x$ under tellurium-vapor. Therefore, the photocurrent of the heterojunction arrays varies sensitively with the changes of shadow so as to perform noncontact detection (**Figure 9**a). With the position of fingers changing, the photoresponse of the different arrays will comprehensibly be processed by microprocessors and thus different operation will be carried out (Figure 9b). This work potentially promotes the arrayed 2D materials into particle use, and demonstrates a possible way to integrate 2D/3D optoelectronic architectures.[180]

Moving forward from the single imaging function of traditional photodetector, Ham et al. developed an analog optoelectronic processor inspired by biological vision, which is composed of a crossbar array of 32 × 32 MoS_2 photo-FETs (Figure 9c,d) and exhibits persistent photoconductivity effects.[181] The FET array is fabricated through the top-down methods. Large-scale MoS_2 film was fabricated through metal-organic CVD. The MoS_2 channel for each pixel was isolated by RIE where mixed gases involving O_2, Ar, and CHF_3 were employed. The optoelectronic processor has high photoresponsivity and photodetection rate, and its photocurrent decays very slowly, enabling a long state retention time. To measure the performance of the FET crossbar arrays, the authors designed the printed circuit boards (PCBs) as illustrated in Figure 9e. The FET arrays keep good consistence in the performance. The authors counted the value of the V_{th} and mobility to demonstrate the variation between devices is relatively small (Figure 9f). Furthermore, the photoelectric processor simulates two main functions of the human vision system: 1) capturing and storing images, 2) processing and recognizing images. It integrates front-end optical image sensing and back-end image recognition in the same material and device platform, showing excellent performance in image filtering, MNIST handwritten number recognition, and other aspects.[181]

Photodiode is another well-developed 2D photoelectronic device.[182] Nanopatterning technologies help the photodiodes of different pixels integrated to a complete image sensor. Mennel et al. fabricated a lateral p-n junction photodiode array that can be used as an artificial neural network (ANN) using several-layer WSe_2 crystal.[183] The authors designed the ICs including N photoactive pixels which contain M subpixels (Figure 9g,h). The WSe_2 layers were mechanically exfoliated from the bulk and transferred on the silicon substrates. EBL process and RIE (Ar/SF_6) were serially applied to obtain 27 pixels based on WSe_2. Due to bipolar conduction behavior and excellent photoelectric performance of WSe_2, the device exhibits adjustable responsivities. The devices were constructed into a 3 × 3 imaging array with three detectors per pixel (Figure 9i). The ANN is tested as a classifier and an autoencoder, respectively, and both show robust and reliable performance.[183]

Nanopatterning technologies also help the artificial vision to move from single synaptic device level to integrated level. Inspired by human vision systems, Hu et al. fabricated 5 × 5 synaptic device arrays based on MoS_2/In heterostructure on quartz hemisphere shell substrate (Figure 9l).[184] Assembled with lens and quartz shelves, the artificial vision system are successfully fabricated (Figure 9m). The MoS_2/In devices exhibited persistence photocurrent with ultralow power consumption. The photocurrent will keep a period time after illuminated by 532 nm laser. Also, with illumination time increased, the photocurrent increases so as to store the exterior information. With the integration density increasing, the stored information will increase so as to obtain distinct image (Figure 9n). The new material systems and novel device structures are flourishing resulting in function extend of image array. The all-in-one concept requires the image sensor could perform data preprocessing and storage which highly depends on the novel device structure realized by nanopatterning.

4. Conclusions and Outlook

We have summarized the most recent nanopatterning technologies for 2D materials, as well as the enabling advanced

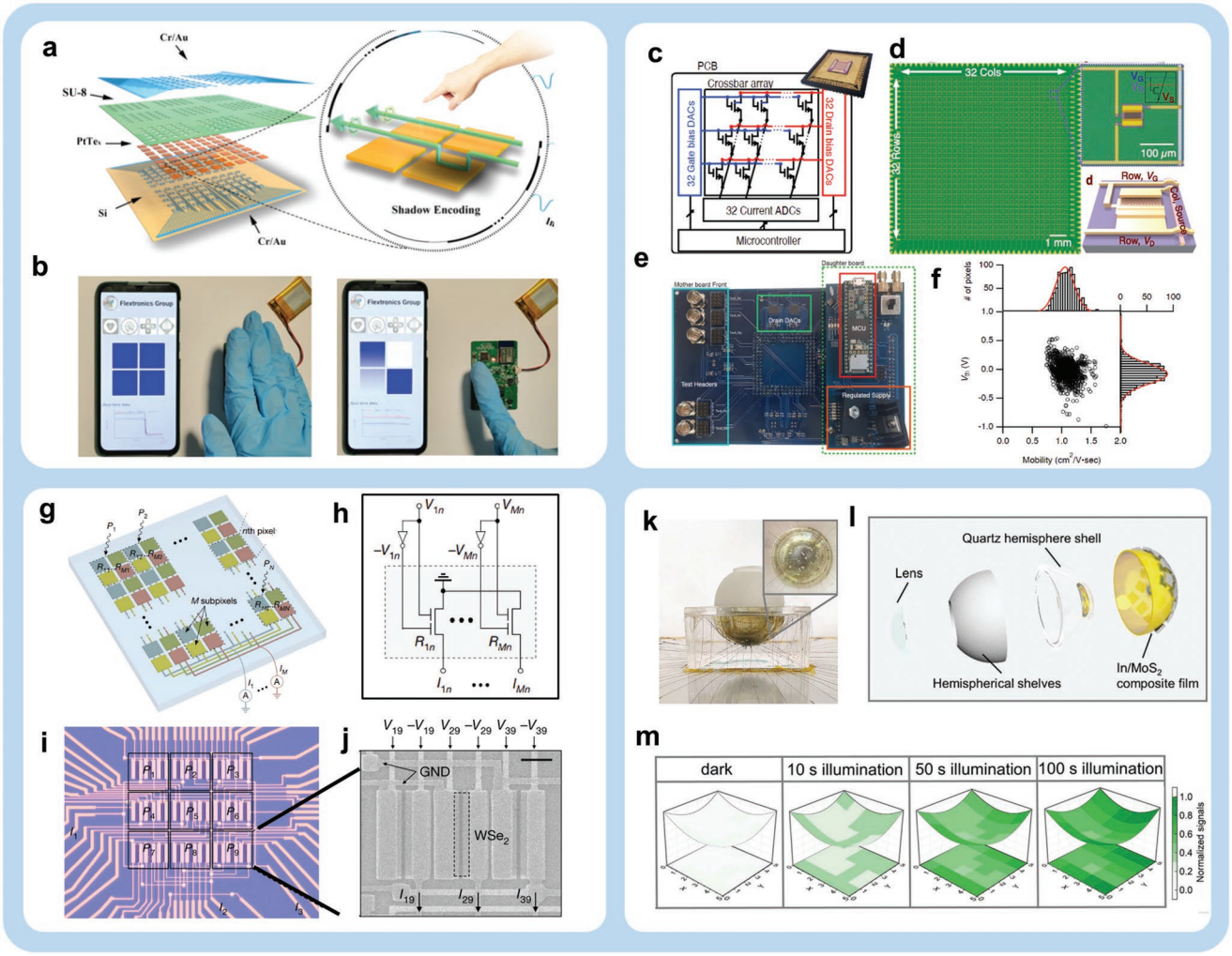

Figure 9. Optoelectronic devices. a) Flexible integration technologies for the fabrication of ONCS based on $PtTe_x$/Si photodetector arrays. b) The operation demonstration of ONCS. a,b) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[180] Copyright 2021, The Authors, published by UESTC and John Wiley & Sons Australia, Ltd. c) Schematic of the MoS_2 optoelectronic processor inspired by the biological vision. d) Lithographically fabricated large-area MoS_2 FET crossbar arrays. e) PCBs for measurement setup. f) Scatter plot of the measured V_t and mobility for the 946 working FETs in the array and corresponding histogram of these two parameters. c–f) Reproduced with permission.[181] Copyright 2020, Wiley-VCH. g,h) Illustration of the ANN photodiode array and circuit diagram of a single pixel in the photodiode array. i) Optical image of the photodiode array, which consists of 3×3 pixels and j) SEM image of one of the pixels. g–j) Reproduced with permission.[183] Copyright 2020, The Authors, published by Springer Nature. k,l) Photo and schematic illustration of the artificial vision system based on 5×5 MoS_2/In arrays. m) Illustrations of the imaging functions under different illumination time. k–m) Reproduced with permission.[184] Copyright 2021, Wiley-VCH.

applications in electronic and optoelectronic devices. The numerous newly emerging research articles in the past few years show us the general way to get nanopatterns of 2D materials, including the bottom-up and top-down methods.[4] The nanopatterning methods are critically dependent on the large-scale synthesis of 2D materials, advanced photolithography, and other precise nanofabrication technologies.[132,149,185] Prompted by these novel technologies, nanopatterns of 2D materials are close to batch production for practical integrated devices.[156] We summarized that not only traditional electronic and optoelectronic devices such as logic circuits, memory devices, photodetector arrays, and photodiodes have been fabricated, but also novel devices including memristors and artificial synapses are reported. We discussed how nanopatterning technologies affect the device performance.

For integrated logic devices, high integration density enables high computing ability. The portable electronics equipment requires the smaller feature size. To meet these demands, nanopatterning technologies with high precision and capable of wafer-scale fabrication are prerequisite. For example, logic gates based on MoS_2 have been developed from single device stage to the wafer integration stage.[48,186] For memory devices, high integration density is the key parameter which determines the memory capacity. Memory crossbar arrays with high integration density will execute more complicated in-memory computing tasks. For instance, the h-BN-based memristor arrays with high integration density are capable of executing large-scale matrix computing.[164] For optoelectronic devices, the demand of miniaturization of optoelectronics devices has emerged which requires the high integration density of devices. However, with

the decrease of the feature size, the edges and defects on the 2D materials will inevitably increase, prominently tuning the band structure. The band structure intensively affects the light–matter interactions. As a result, nanopatterning technologies with high precision and less destruction are critical for integrated optoelectronics.

The excellent device performances reported in these researches well demonstrated that the emerging 2D materials are promising for future electronic and optoelectronic application, of which the development of 2D nanopatterning technologies is of great importance for obtaining high-quality material structures and ultrahigh integration density.[6,148,187] Despite the encouraging developments, the advanced 2D nanopatterning technologies for plant-scale nanofabrication are still immature. For instance, the effective removal of photoresist residues on the surface of 2D materials is a common issue.[121,188,189] The photoresists are inevitably hardened during the RIE process, making their complete removal very tough.[140] In traditional nanofabrication for silicon, high-energy plasma is often employed to remove photoresist residues.[190,191] 2D materials with atomic thin layers are easy to be doped and decomposed by high-energy plasma.[156] It is necessary to exploit new approaches for removal of photoresist residues on 2D materials without damaging the crystal structure.

On the basis of the most recent studies, several techniques are proposed to solve the photoresist contamination problems. First, developing novel all-inorganic photoresist systems provides an alternative way to maintain clean surface of 2D materials. All-inorganic photoresists such as ice[192] are recently reported to show a higher precision than the conventional organic photoresists, which can be easily absorbed on the edge of 2D materials and bring inevitable contamination.[46] In addition, the use of inorganic photoresists effectively avoids organic reactions which may bring defects on the surface of 2D materials.[80,140] Second, inserting a buffer layer between the surface of 2D materials and photoresists can achieve the indirect contact and protect the surface of 2D materials from contamination.[140] For instance, recently Choi et al. utilized the buffer layer to remove photoresist completely and a relatively clean surface of graphene was obtained after RIE.[140] Third, developing resist-free lithography techniques, which directly avoids the possible contact of photoresists, might of great suit for 2D materials.[31] Currently various direct nanopatterning technologies based on mechanical probes and lasers have been successively reported for 2D materials.[141,193] Further development of novel photoresist-free methods with less time consumption and higher precision will be of great promise in the future.

Meanwhile, nanopattern of 2D materials always leads to new physical phenomenon. However, limited by fabricating and patterning methods, many new phenomena are not revealed. For instance, the 3D plasmons are not observed in semimetal $PtSe_2$ since the difficult synthesis of few layers $PtSe_2$ without Se vacancies.[194] Nanopatterning methods of 3D structure for 2D materials are flourishing. For example, the interesting electric properties have been observed in wrinkled MoS_2.[55] Also the rolled TMDs exhibited higher mobility[118] and the spiral TMDs exhibited strong nonlinear optical response.[195] However, application of 3D structures for 2D materials needs further exploring.[203] Though the rolled superlattice is well fabricated, the optical application and electric application are not fully exploited.[119] In the future, the new functionalities caused by nanopatterns will be revealed.

Developing novel nanopatterning technologies to achieve the high-quality integration of 2D materials with the silicon-based devices is another urgent issue to accelerate their practical application.[4,187] The current nanopatterning techniques of silicon are usually incompatible with 2D materials.[185,187] Besides the inevitable contamination during the solvent-based nanofabrication process,[31] the widely adopted mechanical transfer techniques also bring severe structural distortion and damage to the 2D surface.[24,185] The direct growth of 2D nanopatterns on silicon substrates may solve the problem.[156] For instance, the metal precursors for 2D materials can be selectively deposited on the surface of silicon substrate with an atomic clean and sharp interface via a galvanic deposition approach.[196] Followed by sulfurization or selenization, the uniform TMDs could be facilely and directly patterned on silicon. The as-fabricated TMDs protect the silicon surface from further oxidation, ensuring a clean interface between TMDs and the substrates.

Overall, with the continuous progress in wafer-scale synthesis of 2D materials, the subsequent nanopatterning technologies become of critical importance. High-quality and controllable nanopatterning of 2D materials are the most crucial step to promote their practical application from the laboratory scale. More and more attentions should be paid to the progress of nanopatterning technologies for further development of 2D materials. To achieve the batch production with a commercial and industrial standard, more effort needs to be conducted to simplify the production processes, reduce the manufacturing costs, and constantly improve the manufacturing precision. We speculate that advances in nanopatterning technologies of 2D materials will invigorate the semiconductor industry, opening a new era for novel electronics and optoelectronics.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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