Proceedings of the 4th IEEE Int. Conf. on
Nano/Micro Engineered and Molecular Systems
January 5-8, 2009, Shenzhen, China

Low Temperature Direct Bonding for Hermetic Wafer level Packaging

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***Abstract* —A novel hermetic wafer level packaging technology is presented in this paper, which was realized by the aid of low temperature direct bonding. One silicon wafer with etched cavities and the other bare wafer, which acted as cover and substrate respectively, were bonded to demonstrate the feasibility of this technology. The bonding surfaces of both wafers were activated hydrophilically by a series of wet chemical treatments and the data of contact angle measurement showed the activating process was efficient. After prebonding and annealing in 350℃ for 5 hours, the hermeticity and bonding strength of the cavities in bonded wafers were evaluated. The average hermetic performance was 1.175×10^{-8}Pa•m3/s and strength was 7.8Mpa.**

Keywords —***direct bonding; hermatic; wafer level packaging; low temperature;***

I. INTRODUCTION

In integrated circuit (IC) and Micro-electromechanical Systems (MEMS) packaging, devices often need to be encapsulated in micro cavities with vacuum environment or certain atmosphere to achieve special functions. The encapsulation of such cavities could protect devices not only from the hostile external environment for longer lifetime, but also from contaminants for better performance. And the devices encapsulated in micro cavities could have better tolerability during subsequent packaging processing steps (as shown in Fig.1). Therefore, hermetic packaging is widely used in advanced IC and MEMS packaging. Generally speaking, the micro cavities consist of substrate chips and cover chips, which are diced from corresponding wafers and will be bonded together to form encapsulated cavities in subsequent process.

Thus, common hermetic packaging includes many process steps such as singulating, picking & placing, aligning, and bonding, et al. In fact, even normal packaging techniques take up between 75 and 90% of the device costs and as much as 99% of the size [1]. And hermetic packaging will consume more materials, man power, and equipments resources. As a consequence, Hermetic wafer level packaging (WLP) is increasing in importance and still largely under development [2]. In hermetic WLP processing, substrate wafers and cover wafers are bonded prior to dicing. Therefore, hermetic WLP has many advantages [3]. All processing steps are performed at a wafer level resulting in reducing materials and processing cost. Hermetic WLP is truly chip-size packages (CSP) of which package size is the same as a chip size. Therefore, Hermetic WLP is suitable for further miniaturization and lower cost fabrication of electronic packages.

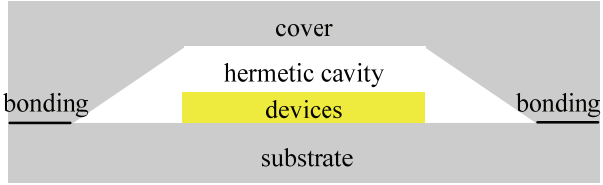

Figure 1. Schematic diagram of hermetic packaging structure

Though there are many bonding methods to achieve hermetic WLP, most of them suffer from high temperature treatment and possible damages to the sealing performance of the encapsulated cavities. It is well known that conventional fusion bonding requires bonding temperature of over 1000℃. On the other hand, solder bonding technology is capable of low processing temperature with reflow of solder and may be applicable to packaging applications. However, flux used in conventional solder to improve wetting capability may cause serious contamination problems for hermetic package [4]. But if the bonding surfaces of substrate and cover wafers are activated properly, all the bonding processing will be accomplished below 350℃. Therefore, by the aid of surface activated direct bonding technique, hermetic WLP could be realized without solder in low temperature.

II. EXPERIMENTS

In order to validate the feasibility of hermetic WLP realized by low temperature direct bonding, demonstrative bonding experiments and corresponding tests were performed.

A. Experiments Design

One wafer with etched cavity acted as packaging cover, which were bonded to another blank wafer to form a hermetic cavity. The wet chemical treatments were carried out to make the bonding surfaces activated hydrophilically and then two wafers were bonding spontaneously (prebonding). After prebonding, wafer pairs were annealed and the bonding interface was inspected. The bonding strength and hermeticity tests were performed as well.

This project was supported by National Key Basic Research Special Found of China (Grant No.2009CB724204), National Natural Science Foundation of China (Grant No. 50805061, 50875103, 50775090 and 50775091), Hi-Tech Research and Development Program of China (Grant No. 2006AA04Z325) and Program for New Century Excellent Talents in University of China (Grant No. NCET-06-0639).

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B. Materials preparation and experimental setup

The silicon wafers used in experiments were 50mm in diameter, 380μm in thick and p-type (100)-oriented. Though wafer with high surface roughness could be bonded by the aid of pressure, it was still polished by chemical mechanical polishing machine (CMP) to smooth the wafer surface. After polishing, RMS of polished wafer decreased to about 0.1nm.

To evaluate the result of surface activation, the contact angles of bonding surface before and after wet chemical treated was measured by a contact angle meter. After prebonding, a quartz tube furnace was applied to anneal wafer pairs to enhance the bonding strength.

The bonding interface within the bonded pairs was inspected by infrared transmission system and the bonded wafer pair was diced to small samples so that cross section could be observed by scanning electron microscope (SEM). And consequent bonding strength test were carried out in an in-house tensile testing machine which was similar to the equipment presented by M.X. Chen [5]. The hermeticity of cavity formed by surface activated direct bonding was measured by a Spectron 5000 Helium Leak Detector from BOC Edward.

C. Experiments procedures

1) Cover wafer fabrication

Before bonding step, the packaging cover was made of a blank wafer. Isotropic etching was chosen to fabricate the cavity and Cr and Su8 multilayer masks were used to improve the protective performance.

- Wafers were cleaned by acetone in supersonic cleaner for 20 minutes and then boiled in SPM (H_2SO_4:H_2O_2=2:1), which removed most organic and metal particle contaminations.
- A 300nm Cr metal membrane was sputtered on the wafer surface, on which a Su8 negative photoresist membrane with 50μm thickness was spun. After a hard baking processing in 150℃ for 30min, Su8 membranes was cured and would be protective mask in consequent HNA etching step.

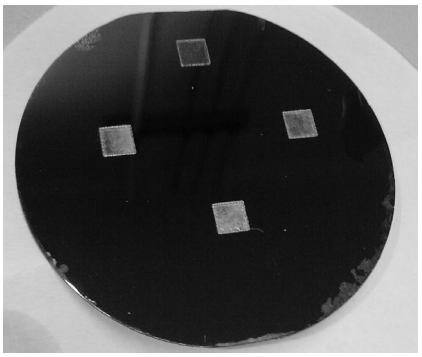


Figure 2. Cover wafer with etched cavities

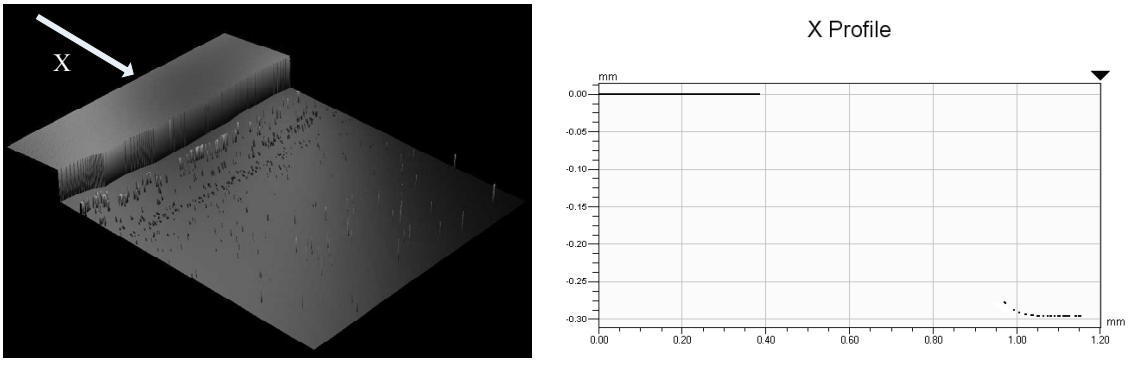
- Wafer with protective mask was put into HNA ($HF:HNO_3:CH_3COOH$=1:1:3) and the backside was covered with a polymer layer to prevent it from being etched in HNA. The etching lasted for 300s.
- After etching, the SPM was used again to remove the Su8 layer for it extremely difficult to be removed with conventional solvent. And on the other hand, hot SPM could also resolve Cr effectively.

The cover wafer with etch cavity was shown in Fig.2 and the side length of the square cavity was 5mm. As shown in Fig. 3, the depth of square cavity was approximated 300μm, which was measured by surface profilometer (the lines in Fig. 3(b) indicted the contour of marginal part, which will be scattered points because in those areas surface roughness is very high so the light beams reflected on those zone could not be received by profilometer adequately).

2) Surface activated direct bonding

After the fabrication of cover was accomplished, all wafers were processed by wet chemical solvents to achieve hydrophilic surfaces.

- Wafers were cleaned by acetone and SPM.
- Dipped in dilute hydrofluoric acid for 30 seconds to remove native oxide layer on surface.
- Dipped in RCA-1 solution (NH_4OH: H_2O_2: H_2O=1:1:5)



(a) (b)

Figure 3. Schematic diagram of hermetic packaging structure
(a) Three-dimensional profile view; (b) Two-dimensional sectional profile of the etched groove in X direction

(a) (b)

Figure 4. Contact angle of (a) untreated surface was 40.46° and (b) activated one was 3.76°

for 15 min at the temperature of 75℃.

- Immersed in RCA-2 solution (HCL: H_2O_2: H_2O=1:1:5) for 15 min at 75℃.

And deionized water flushing was followed each processing. Then the wafers were spin-dried after rinsing. And an infrared light was used to rise the temperature, thus the spin-drying time was reduced. After wafers were spin-dried, contact angle of treated surfaces was measured. Since the contact angle decreased sharply from 40.46° to 3.76° after wet processing (Fig. 4), it is obvious that surfaces hydrophilicity was improved efficiently, in other words, surfaces needed to be bonded were activated successfully.

After hydrophilic surface activated processing, the cover wafer and substrate were put together face to face and the prebonding was accomplished. Then bonded wafer pair was sent into quartz tube furnace to anneal in 350℃ for 5 hours. The annealed wafers pairs were diced to 8×8mm samples and each of them included one cavity. The samples were endured bonding strength test. The gross leak test and fine leak test were preformed according to MIL STD 883E, method 1014.9.

III. RESULTS AND DISCUSSION

A. Interface inspection

For hermetic packaging, voids in bonding interface, which would be interconnecting channels between sealed cavity and external environment are often fatal defects. Therefore it is very important to get void-free bonding interface in hermetic packaging. Since infrared transmission inspection could find the voids in inner bonding interface, the defects in bonding interface within the bonded wafer pairs were inspected by an infrared transmission inspection system. From the image acquired by this system (Fig. 5), voids could hardly be found in the bonding interface. It is implied that there was almost no fatal defects existing in bonding interface.

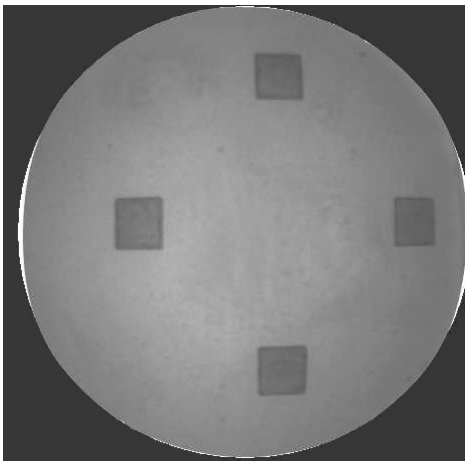


Figure 5. Infrared transmission image of bonded wafer pair

The bonded pairs were cut and made into SEM observation samples. The SEM photo of cross section of bonded area was shown in Fig 6. The bonding transitional layer with the thickness of 241nm was legible and it was even and uniform, which meant that two wafers were bonded densely.

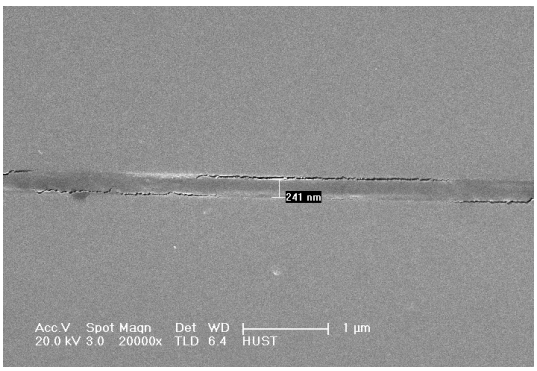


Figure 6. The SEM photo of cross section of bonding interface

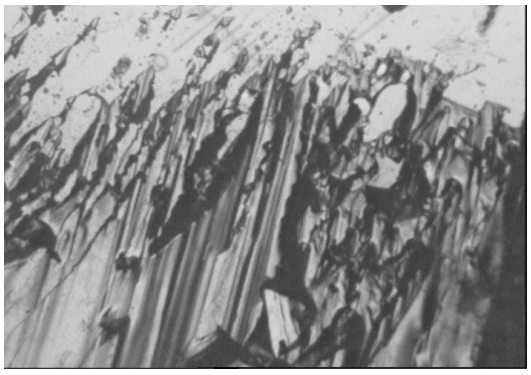


Figure 7. The optical microscope (40×) photo of fracture silicon after bonding strength testing

B. Tensile Strengh

The bonding strength of samples also had been measured and average strength was 7.8Mpa. The scale-like fracture trace in fractured sample (Fig. 7) showed that it was a typical brittle fracture and the crack started not at bonding interface but at the internal silicon wafer. All these indicated that cover wafer and substrate were bonded firmly.

C. Hermeticity Tests

The hermeticity tests were performed according to MIL STD 883E, method 1014.9. Fine leak tests and gross leak tests were carried out successively. All samples showed an average helium leak rate of 1.175×10^{-8}Pa•m3/s, which didn't reach the failure criteria specified in the MIL standard (5×10^{-9}Pa•m3/s). But to civil productions, the hermetic performance at this level is satisfactory.

IV. CONCLUSIONS

Hermetic WLP is a promising technology which can provide a more protective environment for packaged device with improving production efficiency. In this work a novel hermetic WLP technology which was realized by the aid of low temperature direct bonding was developed. Hydrophilic surface activated direct bonding was performed successfully and the temperature of processes all below 350℃. The average hermetic performance was 1.175×10-8Pa•m3/s and strength was 7.8Mpa.

ACKNOWLEDGMENT

The authors wish to acknowledge the Mcirofabrication and Testing Center of Huazhong University of Science and Technology for the preparation and observation of the samples. And division of Micro Optical Electro Mechanical Systems, Wuhan National Laboratory for Optoelectronics is also appreciated for the help of helium leak tests.

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