Porous Light-Emitting Diodes With Patterned Sapphire Substrates Realized by High-Voltage Self-Growth and Soft UV Nanoimprint Processes

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***Abstract*—Nanostructured GaN-based light-emitting diode (LED), with its high performance on light extraction efficiency, has attracted significant attention for the potential application in solid state lighting. However, patterning structures at nanoscale feature size with large area and low cost is of great importance and hardness. In this paper, a 2 inch anodic aluminum oxide (AAO) template was used as the initial mold to copy the photonic-crystal-like structures (PCLSs) on a blue-light LED by soft UV nanoimprint lithography. An additional solute, aluminum oxalate hydrate, is employed to overcome the burn-through issue in the high-voltage anodization which is critical for the fabrication of the large-pore (250–500 nm) AAO. The photoluminescence and electroluminescence enhancements of the patterned LED device with 150-nm-deep PCLSs are, respectively, 45% and 11.4% compared with the un-patterned LED device. A 3-D finite-difference time-domain simulation confirms that the light extraction efficiency is enhanced when PCLSs are formed. The proposed method is simple, cheap, repeatable in large area and compatible with the high volume production lines.**

***Index Terms*—Light-emitting diode (LED), nanoimprint lithography (NIL), optoelectronics, photonic crystal (PC).**

I. Introduction

GaN-based blue-light light-emitting diodes (LEDs) have recently attracted significant attention for their comprehensive applications in vehicle lamps, liquid crystal displays, general illumination, etc. However, the external quantum efficiency (EQE) of LEDs, so far, is still not high enough to realize the LED-based solid state lighting. Theoretically, the calculated light extraction efficiency of GaN-based LEDs is about 7–8% [1], which results in a poor device performance with respect to replacing light fittings. One of the primary reasons for low light extraction is total internal reflection at the interface between a LED device and air. Thus, various attempts have been made to enhance the device performance, such as surface roughening of the p-GaN [2] or indium thin oxide (ITO) transparent electrode layer [3], the use of ZnO nanorod or nanotip arrays [4], [5] and photonic crystals (PC) [6], [7]. Despite the excellent light extraction efficiency of these methods, the nanostructures are usually fabricated directly or indirectly [e.g., nanoimprint lithography (NIL)] through the tedious and time-consuming focused ion beam or electron beam lithography (EBL) methods [8], [9], which conversely limits their potential applications in LEDs.

Since the anodic aluminum oxide (AAO) method was proposed by Masuda and Fukuda in 1995 [10], the triangular-arranged similar PC structure of AAO has been widely used to prepare various optical and optoelectronic devices for its cheap and simple in fabrication. The commercial value outstands in the widespread use of solar cells [11], [12], lenses [13] and transparent polymer [14], etc. Recently, the AAO method has been invited to LED field, and the use of AAO to pattern Si substrate [15], AlN buffer layer [16], un-doped GaN [17], n-GaN [18], [19], p-GaN [20]–[22] and ITO [21], [22] have demonstrated a success for enhancing the light extraction efficiency of corresponding LED devices. Yet, among all these applications adopting AAOs, the direct substrate patterning scheme by Al deposition and subsequent anodization need to remove the Al_2O_3 layer at any single fabrication cycle, thus it fails to meet the repeatable requirement. Moreover, the use of the freestanding AAO as the etching mask layer for pattern transfer encounters the following issues: (a) the Al_2O_3 thin layer is essentially fragile and can't be obtained on large scale; (b) the nonflatness of wafer surface (induced from the lattice mismatch of alumina and epitaxial materials) degrades the pattern transfer uniformity in large area. Although Zhou *et al*. proposed a nanoimprint lithography process to roughen the p-GaN surface for a higher EQE [20], the surface nonflatness and filling-speed difference of AAO will lead to the feature size loss and fails to obtain the honeycombed nanopore structures on target substrate [23]. Besides, these attempts are only performed on LEDs with flat sapphire substrates, and it

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is important to note that achieving high internal quantum efficiency is also important for realizing InGaN-based LEDs with high EQE. Most high quality blue-light LEDs are fabricated on patterned sapphire substrates (PSSs) in the current LED industry since the threading dislocation density in the epitaxial GaN layer is effectively reduced by the epitaxial lateral overgrowth and the PSS (both micro-scaled and nano-scaled) act as scattering centers for the guided light inside LED devices [24]–[27]. Furthermore, one should notice that all the PC structures used in LEDs have a structure dimension comparable to the emission wavelength (450 nm, blue light) for optimizing the light extraction efficiency of corresponding devices [28], [29]. While in the self-organization field, AAO with such large-scale nanopore remains difficult to be fabricated [30], [31]. Therefore, to find a simple, effective and repeatable method for surface patterning with hundreds-nanometer nanostructure for further enhancing the light extraction efficiency of GaN-based LED with PSS is of great importance and value.

In this study, photonic-crystal-like structure (PCLS) is formed on the GaN-based LEDs, fabricated on the PSS, in order to increase the EQE by soft UV-NIL, which offers low cost and high throughput compared to other lithography techniques such as photolithography, EBL and so on. AAO with nanopore dimension comparable to the blue-light wavelength, fabricated under a high pressure of 185 V, is invited as the initial template of NIL for the first time. The electrical and optical properties of the patterned LED devices with PCLS are confirmed by the test and simulation results.

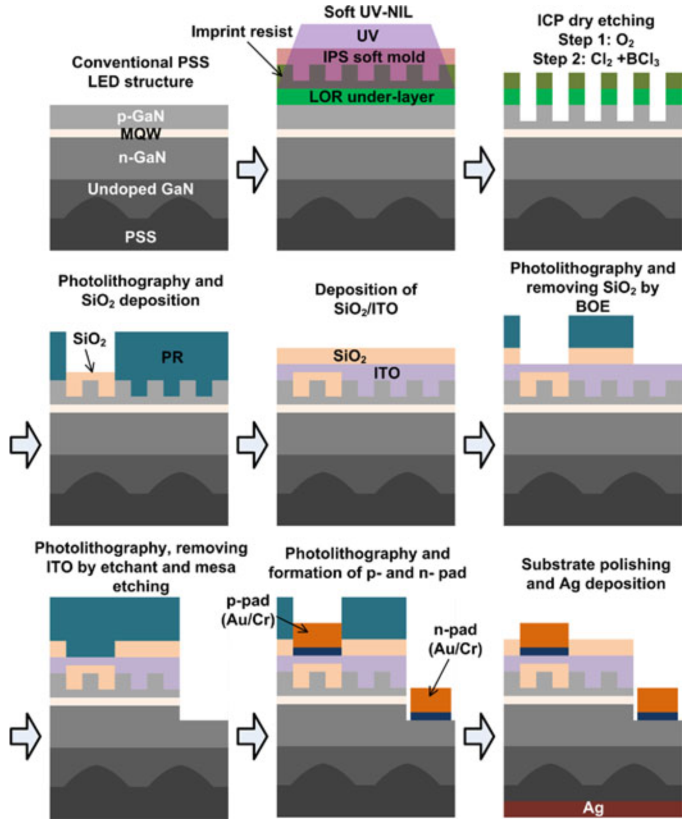

Fig. 1. The fabrication process of the patterned LED device with PCLS on the p-GaN layer of the GaN-based LED by using NIL and etching processes.

II. Device Fabrication

A typical GaN-based blue LED structure was grown on a (0001)-oriented PSS by a conventional mental organic chemical vapor deposition process. After the deposition of a thin low-temperature GaN buffer layer, the LED structure, which consists of layers of 2.5-μm-thick un-doped GaN, 2.5-μm-thick n-GaN, 72-nm-thick InGaN/GaN multiple quantum wells (MQW) and 200-nm-thick p-GaN, was fabricated.

Fig. 1 shows the overall patterning process for the fabrication of the PCLS pattern on the LED structure. First, a 100-nm-thick LOR (an under-layer resist, purchased from Microchem) sacrificial polymer layer was coated on the p-GaN surface, followed by a soft UV-NIL process at 20 bar of pressure while exposing the stack of the mold/resin/LED wafer to UV for 60 s. The energy for polymerization of UV resist and the energy density of UV source are 22.5 and 35 mW/cm^2, respectively. In the soft UV-NIL process, a soft IPS mold was used for conformal contact with the LED wafer. The soft IPS mold was obtained via the thermal NIL by using AAO as an initial mold. Detailed fabrication parameters of the soft UV-NIL and subsequent inductive coupled plasma (ICP, Oxford Plasmalab 100 system) dry etching can be seen in our previous works [23], [32]. After the dry etching process, the sacrificial polymer layer under the imprinted pattern was cleared off with acetone to reveal the PCLS patterned p-GaN surface on the LED structure. To fabricate the LED devices, a photo-resist was coated onto the patterned LED wafer and was partially removed by photolithography to establish the contact region for p-GaN. Then, a 100-nm-thick SiO_2 was deposited as the confinement layer for p-contact. Next, a 150-nm-thick ITO and 235-nm-thick SiO_2 layer was deposited after removing the photo-resist. Prior to mesa etching, p-GaN PCLS patterns on the contact region for p- and n-GaN, which is not covered with the photo-resist, were removed along with the underlying SiO_2 layer by dipping the sample in buffered oxide etcher solution. Through mesa etching using ICP and deposition of p-pad, n-pad and omni-directional reflector (ODR) metals, the 300 μm $\times$ 300 μm lateral-type LED devices were fabricated.

To analyze the optical and electrical properties of the patterned LED devices, measurements of photoluminescence (PL), electroluminescence (EL) and $I-V$ characteristics were conducted. A 3-D finite-difference time-domain (FDTD) simulation on light extraction of the patterned LED structures was carried out using the Rsoft software with its FullWAVE functional module [33], [34].

III. Experiment Result and Discussion

The AAO is fabricated from the well-known two-step anodization process. According to the proportion relationship between the pore dimension and the applied anodization pressure [35], a voltage above 160 V is necessary for obtaining nanopore size which is similar to the wavelength of blue light in aluminum anodization process. However, the high pressure

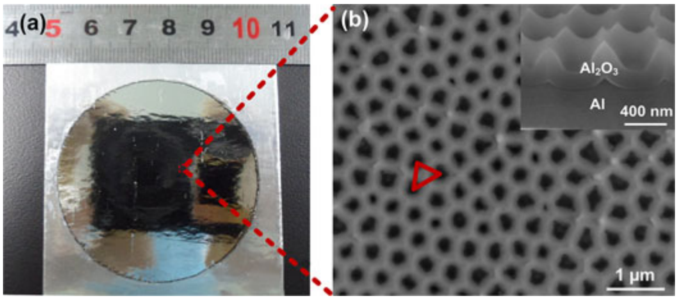

Fig. 2. (a) Photography and (b) SEM images of the 2 in AAO. The AAO is fabricated in a 1 wt% H_3PO_4 + 0.01M $Al_2(C_2O_4)_3$ mixture solution under the temperature of 5 °C and the voltage of 185 V. The first and second anodization times are 2 h and 10 s, respectively.

anodizations usually burn through the samples and fail to form the self-organized structures [30], [31]. In our experiment, an additional solute, aluminum oxalate hydrate, is employed to slow down the electrochemistry reaction. A shorter second anodization process is used to increase the effective pore depth through the volume expansion of aluminum to alumina. After the anodization process, the sample is dipped into a 5 wt% H_3PO_4 liquid solution for 5 min under the temperature of 60 °C to obtain the desired pore dimension for subsequent NIL process. Fig. 2 is the scanning electron microscope (SEM, Nova NanoSEM450, FEI) image of the as-fabricated AAO. As shown, the nanopore distribution represents a similar triangular lattice arrangement with the average pore period and pore depth of ~493 and ~190 nm, respectively.

Fig. 3 is the SEM images of the patterned resist and p-GaN. In the soft UV-NIL process, pressure-assisted molding technique is applied to ensure the complete filling of the nanostructures [36]. Before soft UV-NIL, A surface treatment was performed by immerging the RN Si mold into a 0.6 mmol/mL 1H,1H,2H,2H perfluorodecyltrichlorosilane/isooctane solution for 10 min for anti-adhesion [37]. Then it was cleaned with isooctane, acetone, IPA and water, and at last blown dried. The nanopore distribution of Fig. 3(a) is consistent with that of the Fig. 2(b), which demonstrates a success by using soft UV-NIL combined with AAO for surface tailoring. Besides, one can easily observe from Fig. 3(b) that the sidewall of the nanopore represents an arc-like profile. As a matter of fact, this arc-like profile can be used to fabricate PC patterns with variable duty cycle via one single initial mold [32]. Our previous work [23] shows that the native nonflatness of the AAO surface is ~100 nm, thus using AAO with nanopores depth lower than 100 nm can't realize the success pattern transfer for both the higher and lower parts. Although one can overcome the influence of nonflatness by increasing the second anodization time to obtain a deeper AAO nanopore, for the commonly used AAO (usually with a nanopore dimension of sub-100 nm), the mechanical strength of the soft IPS nanorod is too weak to serve as a good imprinting mold for NIL. While in this study, the use of ~190-nm-deep AAO demonstrates a success for substrate patterning. After ICP dry etching and removing the LOR under-layer, the PCLS patterned p-GaN is shown in Fig. 3(c). It should be mentioned that the PCLS patterns in Fig. 3(c) is obtained due to the following reasons: 1) large

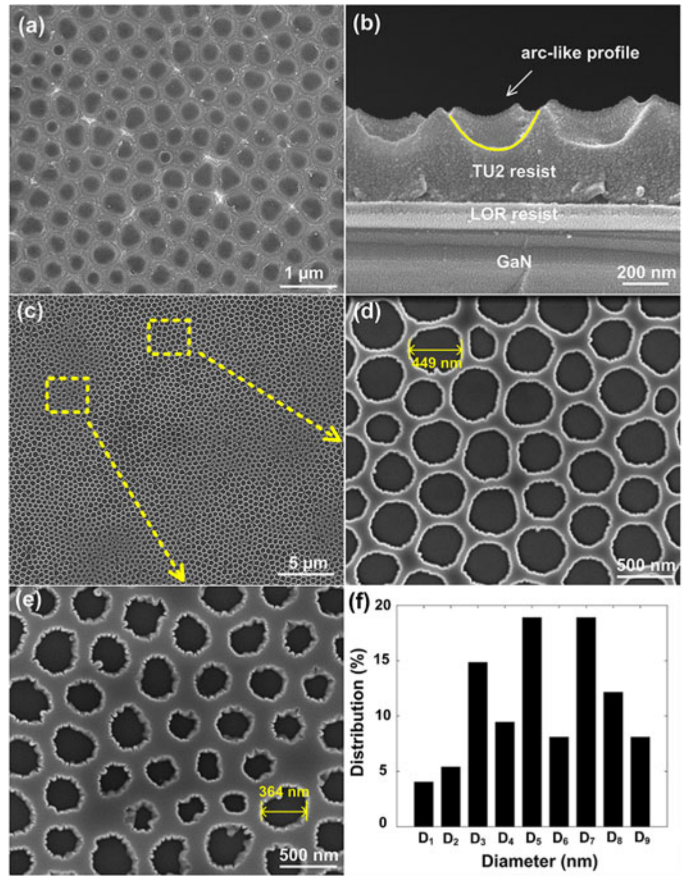

Fig. 3. (a) Top and (b) cross-sectional SEM images of the imprinted resist. (c)–(e) are PCLS patterned p-GaN. (f) Size distribution of the nanopores on p-GaN. The domain of 126–449 nm is divided into nine equal-interval parts $(D_1 - D_9)$ with the increment of 35.9 nm.

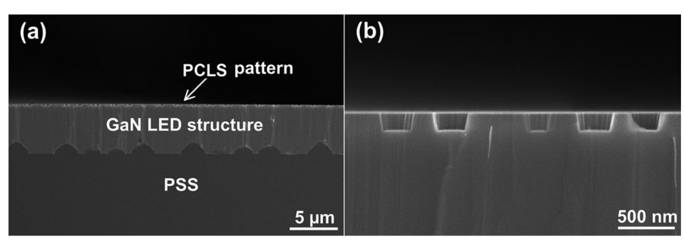

Fig. 4. (a) Low and (b) high magnitude SEM images of the LED device with the PCLS pattern times are 2 h and 10 s, respectively.

nanopore AAO is used, thus the pore depth can be deep enough to overcome the critical depth requirement while maintain the mechanical stability of the soft IPS mold in the soft UV-NIL process; 2) because of the nonflatness of the AAO and the arc-like profile of the nanopore sidewall, nanopore dimension will vary from the higher parts to the lower parts (the lower parts will have a larger pore diameter to the higher ones) after removing the residual resist. Consequently, the largest nanopore diameter decreases from ~449 nm (Fig. 3(d)) to ~364 nm (Fig. 3(e)). Anyway, the proposed method demonstrates a success for direct p-GaN PCLS fabrication via NIL for the first time. Fig. 3(f) shows the size distribution of nanopores in Fig. 3(c) with a mean diameter of 303 nm. Fig. 4 is the cross-sectional images of the GaN-based LED structure with the PCLS pattern, which is grown on the PSS with a diameter of 3 μm, a period of 3.2 μm and a height of 1.6 μm. As shown, the array of PCLS patterns is uniformly fabricated on the p-GaN layer of the GaN-based LED with a pore depth of $\sim$150 nm.

In order to confirm the effect of the presence of PCLS patterns on the light extraction of the LED devices, which were fabricated on the PSS, we measured the PL intensities, the $I-V$ characteristics and EL intensities of the un-patterned LED device and the patterned LED devices with PCLS patterns, as shown in Fig. 5. In Fig. 5(a), the PL enhancements of the PCLS patterned LEDs with nanopore depth of 100 and 150 nm to the one without PCLS are 35% and 45%, respectively. When 20 mA of current is injected, the EL intensities of the LED devices with PCLS patterns of 100 nm and 150 nm in depth were increased by 7.8% and 11.4%, respectively, compared to that of the un-patterned LED device, as shown in Fig. 5(c). The enhancement exhibits obvious advantage compared with that of 10.9% in previous research on LED without PSS [20] since the light extraction efficiency is already enhanced by the PSS. It should be mentioned that the average relative errors of the forward voltages of 100- and 150-nm PCLS patterned LEDs to the un-patterned one in Fig. 5(b) are both below 0.1%. Thus, the electrical properties of the patterned LED devices with PCLS were not degraded since no extra contact resistances were induced.

To investigate the effect of the presence of the PCLS patterns with different depths on the light extraction of LED structures, a 3-D FDTD simulation is conducted. Fig. 6(a)–(c) is schematic diagrams of the simplified model of LED structures for the FDTD simulation. All of the structure parameters are taken from the data mentioned above. The plane of continuous polarized dipoles is placed at the MQW below the GaN surface as the light source which emits photons in random directions and the wavelength of the light source is set to 450 nm. The absorption coefficient of the GaN is assumed to be 300 cm^{-1}, corresponding to a photon life time of 320 fs [29]. The area of the simulation domain is limited to 3.2 μm $\times$ 5.5 μm and only the 400-nm-thick sapphire layer is partially involved in the simulation domain, in order to avoid the FDTD calculation being hugely time consuming. Three different LED structures, consisting of a LED on a flat sapphire substrate, a LED on PSS and a PCLS patterned LED on PSS, are considered as shown in Fig. 6(a)–(c). The cone-like-shaped PSS pattern in the simulation is obtained by tapering the diameter according to the proportion coefficient 1-Z^2, where Z is the normalized height which has a positive value from 0 to 1. The depth of the PCLS pattern is split into levels from 100 to 300 nm with an increment of 50 nm in the simulation. The grid size of the FDTD is set to 10 nm for reliable simulation computation, periodic boundary conditions are applied to the *xy* plane in order to minimize the effect of the small size of the simulation domain and a symmetry boundary condition is applied to the z bottom plane for ODR.

Fig. 7 presents the results of the FDTD simulation for the considered LED structures, which are described in Fig. 6. By inserting the PSS into the normal LED structure, the light extraction efficiency is increased by 19.0%. This agrees well with

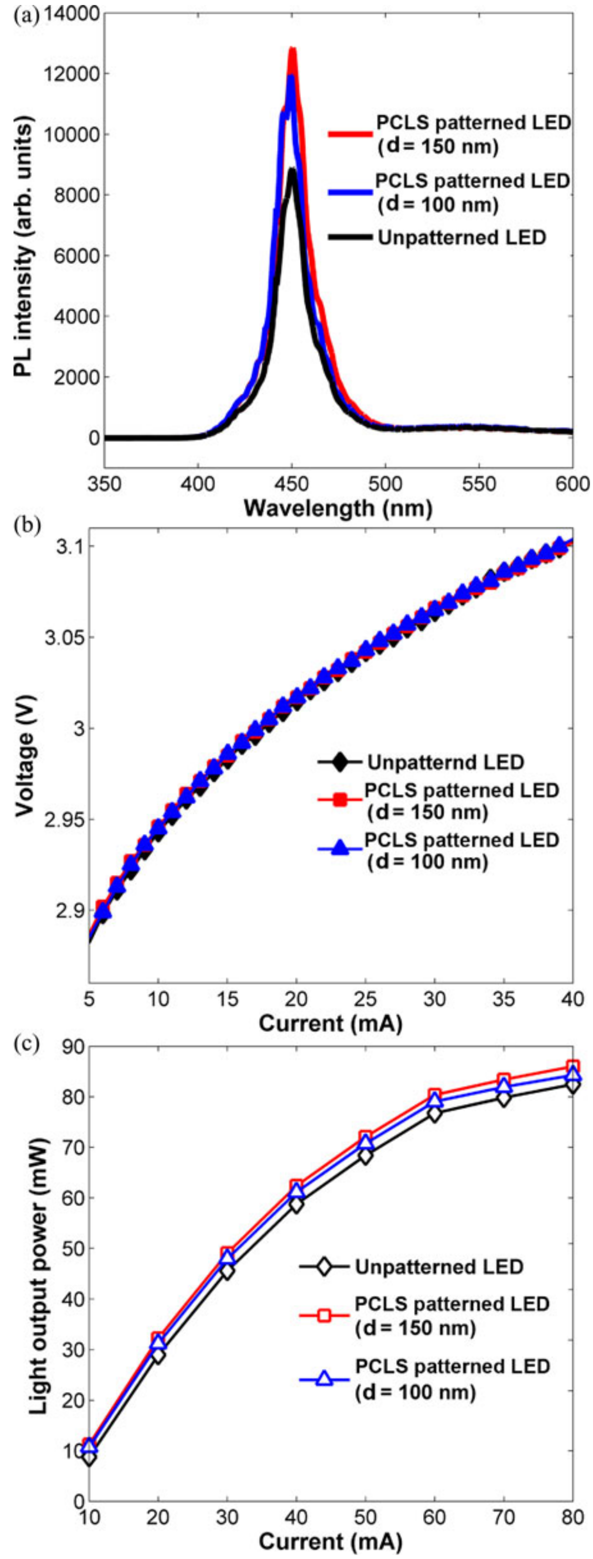

Fig. 5. (a) PL intensity versus wavelength for un-patterned LED device and the patterned LED devices with PCLS patterns of 100 and 150 nm in depth. (b) $I-V$ characteristics of the un-patterned LED device and LED devices with PCLS patterns. (c) Light output power versus injection current for the un-patterned LED device and the patterned devices with PCLS. All LED devices are fabricated on the PSS.

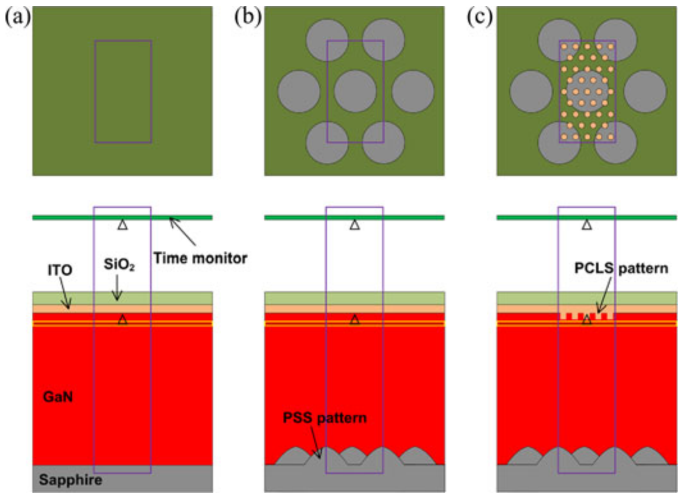

Fig. 6. Simplified FDTD simulation designs of (a) the conventional LED, (b) the LED with PSS and (c) the LED with PCLS patterns and PSS.

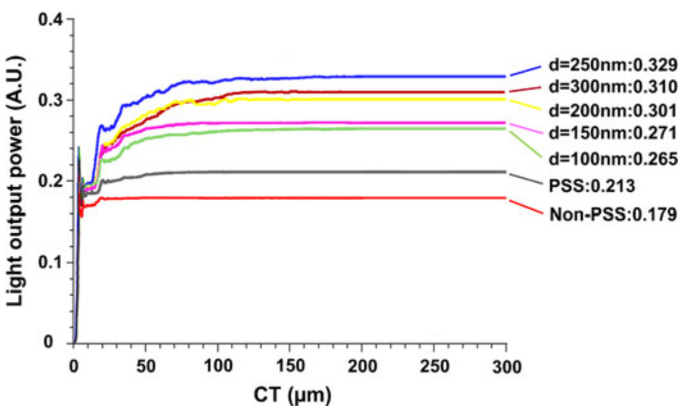

Fig. 7. FDTD simulation results on light extraction of the conventional LED, the LED on the PSS and the PCLS patterned LED with PSS. The thickness of p-GaN is 400 nm for $d = 200$, 250, and 300 nm.

lots of reports that a PSS is helpful in enhancing the light extraction of LEDs, as well as improving the crystal quality of GaN by reducing the threading dislocation density. Comparing with the LED with PSS, the enhancements of $d = 100$ nm (24.4%) and $d = 150$ nm (27.2%) show the same tendency with that of the test results in Fig. 5. Further enhancement will be gained by increasing the depth of the PCLS. When the PCLS pattern with 250 nm of depth is formed on the p-GaN top layer, the light extraction efficiency is increased by up to 54.5%. Thus, from the simulation and test results, we confirmed further enhancement in the light extraction of a GaN-based LED on a PSS by introducing the PCLS patterned layer. This simulation method did not take into account the photon recycling and reabsorption process, thus this method may not provide the accurate absolute value of the light extraction efficiency. However, the use of this method is sufficient for providing comparison of the light extraction of the light extraction efficiency among all the LEDs.

So far, most studies on the light extraction of LEDs have been performed on LEDs with time-consuming (e.g., EBL) or un-repeatable (e.g. direct AAO mask layer) pattern transfer process. Furthermore, enhancing the light extraction of LEDs on PSS is relatively more difficult than it is for LEDs on flat sapphire substrates since the light extraction efficiency is already enhanced by the PSS. However, further increase in the light extraction of the LED device on the PSS is confirmed by inviting soft UV-NIL for forming the natural self-organized PCLS patterns, which suppress the total internal reflection. At every injection current, the patterned LED devices with PCLS showed higher EL intensity than the un-patterned LED devices. The proposed nanofabrication process by using soft UV-NIL combined with AAO is compatible with the semiconductor manufacturing industry and can find its application in various fields, such as outdoor self-clean [11], solar cells [11], [12], sub-wavelength anti-reflection [11], [38] and surface plasmons laser [39]. As a matter of fact, the size of AAO, such as the pore diameter, the pore depth, and the interpore distance, can be easily tuned by the experimental conditions [35], [40]. Further enhancement of the light extraction efficiency of GaN-based LED can be achieved by optimizing the nanopore duty cycle, depth and regularity of the PCLSs as well as the surface flatness of the AAO.

IV. Conclusion

We successfully fabricated a 2 inch AAO with nanopore dimension of hundreds nanometer by inviting an additional aluminum oxalate hydrate solute to the high voltage anodization. Pattern transfer via the as-fabricated AAO demonstrated a success for direct tailoring the p-GaN surface of a GaN-based LED grown on PSS. The PCLS patterned p-GaN represents a triangular-arranged nanopore distribution with the nanopore diameter of 126–449 nm. Enhancement in the light extraction of a GaN-based LED on a PSS by introducing the PCLS patterned p-GaN was confirmed by the test and simulation results. The PCLS patterned LED device on the PSS showed an increase in EL intensity of up to 11.4% compared to an un-patterned LED device on the PSS at 20 mA drive current. This method is simple, cheap, repeatable in large area and compatible with the high volume production lines.

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