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Low Temperature Direct Bonding Technology for Wafer-scale Integration and Packaging

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***Abstract*—A spontaneous low-temperature bonding process was developed for silicon wafer direct bonding. Experiments were conducted to investigate critical process parameters with blank silicon wafers at 120℃. The effects of interfacial micro/nano-scale roughness on bonding were mainly considered. The results showed that different interfacial roughness may lead to three bonding possibilities, namely spontaneous bonding without voids, spontaneous bonding with voids, and bonding with gap under external pressure or un-bondable. The application of the spontaneous bonding process to patterned wafers was also conducted successfully, which shows that the technology will have potential applications in wafer-scale integration and packaging where high temperature and high pressure environment is prohibited.**

Keywords-low temperature; wafer direct bonding; integration; packaging

I. INTRODUCTION

Due to stress-related reliability issues and possible deformation of patterned wafer interfaces under high temperature, high pressure and bonding with intermediate layers involved in the bonding process, low temperature wafer direct bonding can find more industrial applications where high temperature environment (over 450℃) is prohibited [1]. There are several low temperature bonding methods, such as plasma-activated wafer bonding, vacuum wafer bonding and wet chemical activated bonding. Among them, the first two approaches require expensive equipments therefore the process cost is relative high, while wet chemical bonding approach is relative low cost method. Spontaneous wafer bonding is described as a special phenomenon from which the bonded area can be seen spread over the entire wafer surface, particularly for hydrophilic wafer bonding without pressure, which is an ideal bonding technology for low temperature direct bonding [2]. Wet chemical activated bonding can render the wafer surface with hydrophilic properties. However, spontaneous bonding mechanisms still remain poorly understood with regard to their interfacial properties [3]. We address here the problem of spontaneous wafer bonding in relation with the properties of wafer surfaces under low temperatures (less than 200ºC) [4]. Blank silicon wafers with different interfacial properties, such as surface microroughness, were used as an experimental system to investigate low temperature bonding mechanism. The developed process was also applied to wafer-scale packaging where wafers with various patterns were bonded between wafer interfaces.

II. EXPERIMENTS OF BLANK-WAFER BONDING

Low temperature blank-wafer direct bonding can be realized with the aid of pressure [5], however, sometime the pressure is restricted in the process, and spontaneous pressure-free bonding is a solution to this case. Spontaneous bonding is very much related with the interfacial chemical and physical properties, such as hydrophilic surfaces and interfacial microroughness [6]. In our experiments, single-side polished p-type (111) standard wafers in thickness of 380μm were applied for bonding experiments. However, different surface roughness was controlled by polished for comparative experimental study. Generally, the following procedure was applied to the bonding process development, and Fig. 1 shows the schematic of the process flow, where the critical activation process can be either realized by wet chemical solutions or by dry ion sources such as plasma or UV light through surface radiation.

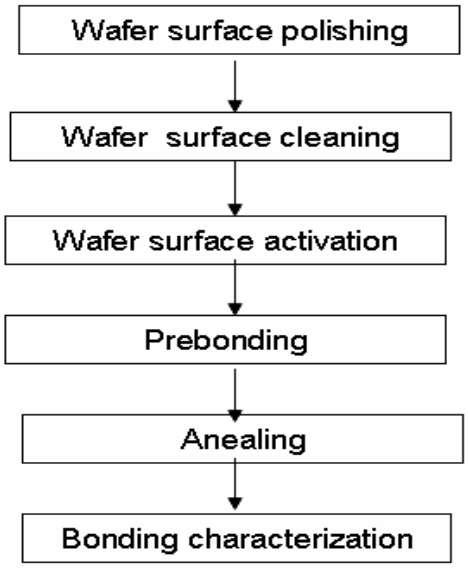

Figure 1. Process flow for low temperature wafer direct bonding

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A. Wafer surface polishing

The surface roughness root -mean-square (RMS) of raw wafer was around 5nm, and it was polished to get lower roughness which was characterized right after the polishing. The results were presented and compared in the later section together with their bonding results.

B. Wafer surface cleaning and activation

Wafer surfaces were processed with following wet chemical treatment procedure to activate and achieve hydrophilic surface.

- Wafers were cleaned by acetone in supersonic cleaner for 20 minutes, which removed most organic contaminations.
- Boiled in mixture of hydrogen peroxide and sulfuric acid (H_2SO_4:H_2O_2=2:1) for 20 minutes. This eliminated metal particle contaminations.
- Dipped in dilute hydrofluoric acid for 30 seconds to remove native oxide layer on surface.
- Immerged in hot nitric acid at temperature of 110℃ for 15 minutes.

And deionized water flushing was followed after each step. After this process, It was observed that contact angle over wafer surface was reduced evidently, in other words, the surfaces of wafers became hydrophilically. Then the wafers were spin-dried after deionized water rinsing for the next prebonding step.

C. Prebonding and annealing

Soon after spin-dried, two wafers were put into intimate contact immediately. If the surface roughness is relative high, bonding wave propagating phenomenon could not happen spontaneously. In the experiments, relative lower surface roughness was applied, spontaneous bonding was reached and then all wafer pairs were annealed in air for 5 hours at around 120℃.

D. Bonding characterization

After the annealing, wafer pairs were inspected by infrared inspection system and the cross-section of bonding interface was observed under a scanning electron microscope (SEM). The results were presented and compared in next section.

Bonding strength is a very important factor related to bond quality and reliability. High bond strength indicates that a good bond had been achieved. Therefore, after annealing, bonded pairs were diced into about 5mm×5mm die for tensile strength measurement. An in-house tensile testing machine was used for this purpose.

III. RESULTS AND DISCUSSIONS

In this study, following the same bonding procedure, such as cleaning and activation process, prebonding and annealing temperature, wafer surface microroughness was controlled to study the requirements and bonding results of spontanesous bonding process. The microroughness was considered as one of critical factors for the formation of spontanesous bonding in the end. Since wafer venders provide typical commercial wafers with roughness RMS around 5.00nm, commercial wafers must be polished to decrease wafer surface roughness. In the experiment, two sets of surface roughness were prepared after polishing, and atomic force microscope (AFM) images of these wafer surface profiles with different roughness were presented in Fig. 2, where RMS was around 0.126nm and 2.229nm separately. From Fig. 2, where left side image was for lower surface roughness, it can be seen that lower surface roughness shows much smooth surface and shows better chances for two surface to contact intimately. These images also can explain why surface roughness was critical for spontaneous process and to what extent the spontaneous process to take place.

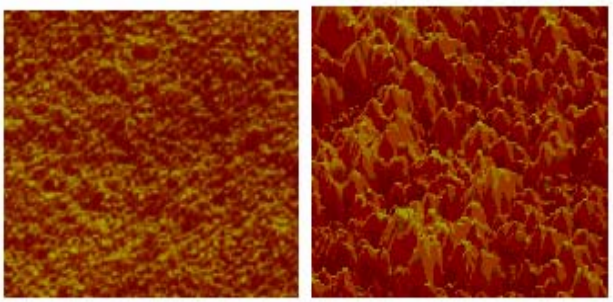

Figure 2. AFM image of surface for silicon wafer with scan area of 2X2μm², Left: image for RMS of 0.126nm; Right: image for RMS of 2.229nm

In the activation process, specially prepared chemical formula was used and strict process parameters such as temperature, time period were obeyed to activate the surface hyropilically, in the meantime, not to destroy the surface roughness. In the prebonding step, bonding took place spontanesous without external pressure. In the annealing step, annealing temperature controlled here was around 120℃. The temperature was much lower compared with typical high temperature bonding process (over 450℃) and the process is considered as low temperature wafer direct bonding process. Overall, the whole wafer bonding procedure is regarded as low temperature spontaneous wafer direct bonding process.

Bonding results such as interface voids and interfacial bonding thickness were characterized for different wafer surface roughness. The experimental results were presented and compared in Table 1 as showed in the following. From table 1, results of three-group of wafers A, B and C with different surface roughness were compared, where commercial wafers in group C with root mean square (RMS) roughness of 5nm were not bondable. The wafers in group A and B showed spontaneous bonding phenomena while voids were detected with infrared (IR) camera at bonded interface for wafers from group B. Another important data was the bonding strength, for the spontaneous bonding process, it can reach as high as 3.5MPa with tensile strength testing.

TABLE 1. LOW TEMPERATURE BONDING FOR DIFFERENT BATCH OF WAFERS

Wafer pair	*RMS (nm)*	*Prebonding process*	*Interfacial thickness (nm)*	*Interfacial voids#*
A	0.126	spontanesous	40	Not detected
B	2.229	spontanesous	100	Detected
C[+]	5.000	not bondable	N/A	N/A

[+]commercial 2inch, P-type, 1-side polished, (111) silicon wafer with thickness of 380μm, #voids were inspected with IR camera.

From Table 1, it showed that the success of spontaneous prebonding process relied on the wafer surface roughness, it also showed bonding quality relied on wafer surface roughness. Besides bonding strength, bonding interfacial thickness and number of interfacial voids were also used to characterize the bonding quality. Generally, the lower the wafer surface roughness, the thinner the bonding thickness, the less possibilities to detect interfacial voids. And the conclusions were illustrated in Fig.3 and Fig.4, where typical image results of bonding interfaces were showed.

As shown in Fig. 3, the typical field SEM images of interfacial thickness for bonded wafers, for RMS of 0.126nm wafers, interfacial bonding thickness was smoother and thinner, comparing with the bonding pairs with RMS of 2.229nm.

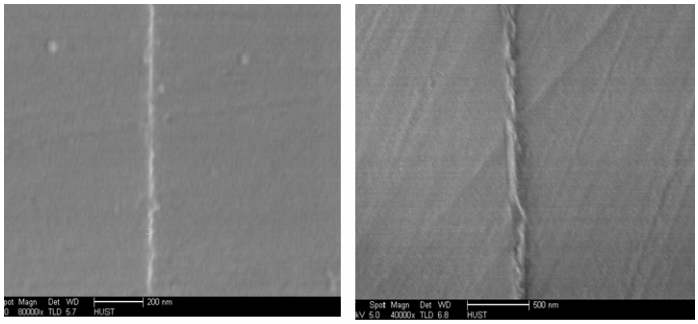

Figure 3. Field-SEM image of bonded interfaces, Left: bonded wafer with RMS of 0.126nm, Right: bonded wafer with RMS of 2.229nm.

As shown in Fig. 4, the typical infrared images of bonded interfaces to inspect voids after bonding, quite some small and big voids were detected for bonded wafers with surface roughness RMS of 2.229nm, while the one with lower RMS of 0.126nm showed little voids. It was obvious that surface roughness was one of most critical factors for the formation of voids after bonding. In order to better control the bonding quality, lower surface roughness was required even spontaneous bonding process may take place during low temperature bonding.

Generally speaking, low-temperature silicon wafer direct bonding process depends on process parameters and wafer physical properties. Different interfacial roughness may lead to different bonding results, namely spontaneous bonding without voids, spontaneous bonding with voids, and un-bondable. Among all factors, wafer interfacial roughness is the decisional factor for both the success of spontaneous bonding and the better quality of the bonded interfaces, although the limit of requirement for roughness has not decided yet.

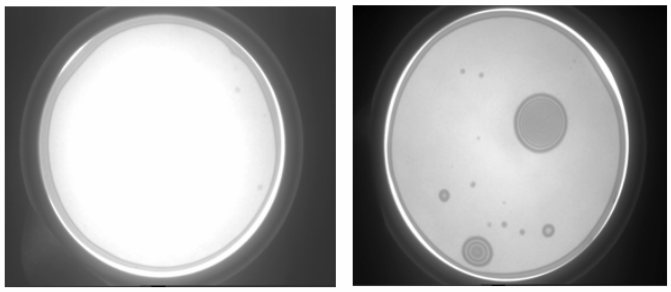

Figure 4. Infrared image of bonded interfaces, Left: bonded wafer with RMS of 0.126nm, Right: bonded wafer with RMS of 2.229nm.

IV. APPLICATION TO WAFER –SCALE PACKAGING

As illustrated in previous section, a low temperature spontaneous bonding process was developed for silicon wafers. Critical factors were presented in the results for the process. Therefore, to application of the technology to wafer-scale packaging and integration for device or system fabrication, process and material requirements have to be obeyed.

In this study, the bonding of patterned wafers was conducted by applying above technology. To illustrate the process for wafer-scale applications, the fabrication of microfludic system was demonstrated. First, micro-channels for fluid flow and cavities for fluid accumulation were fabricated on one blank wafer by etching. Then another blank wafer was bonded directly to seal the micro-channels and cavities following surface cleaning, activation, prebonding and annealing process. It showed that spontaneous bonding process took place during prebonding step and final result was shown in the following Fig. 5. As shown in Fig. 5, no voids were detected using IR system after bonding. Further work is still going on to quantify the bonding results. The work will help the fabrication of microfluidic system in wafer-level and also to other wafer-scale packaging and integration applications.

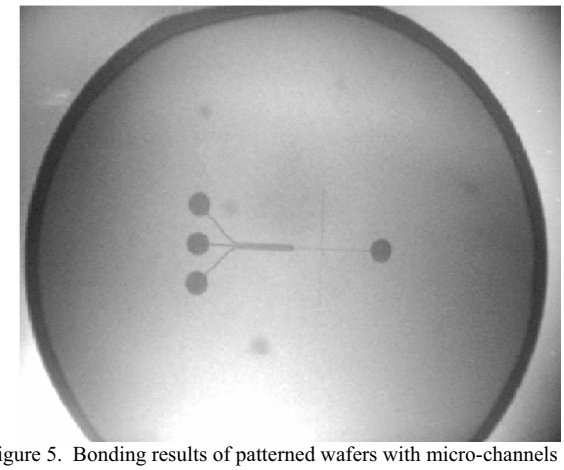

Figure 5. Bonding results of patterned wafers with micro-channels and cavities

V. CONCLUSIONS

Low temperature wafer direct bonding is one of the critical technologies for micro/nano fabrication and wafer-scale packaging. A spontaneous low-temperature bonding process with temperature around 120℃ was developed for silicon wafer direct bonding. Experiments were conducted to investigate critical process parameters with blank silicon wafers. The effects of interfacial micro/nano-scale roughness on bonding were mainly considered. The results showed that different interfacial roughness may lead to three bonding possibilities, namely spontaneous bonding without voids, spontaneous bonding with voids, or un-bondable. The application of the spontaneous bonding process to patterned wafers was also conducted successfully for fabrication of wafer-scale microfluidic system, which shows that the technology will have potential applications in wafer-scale integration and packaging where high temperature and high pressure environment is prohibited.

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