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Article

Direct Monitoring of Nanoscale Deformations across All Layers in Three-Dimensional Stacked Structures

Xiangyu Zhao, Hao Jiang, Jiamin Liu, Changqing Liu, Hui Deng, Renjie Zhou, Nicholas X. Fang, Shiyuan Liu,* and Jinlong Zhu*

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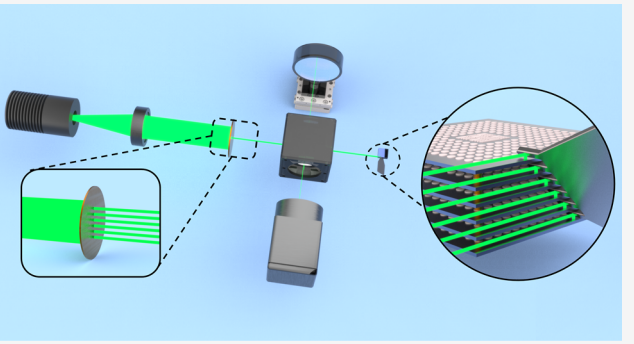
ABSTRACT: Due to its high bandwidth, low latency, low power consumption, and compact size, three-dimensional (3D) integration of semiconductor chips holds the promise of boosting the performance of integrated circuit systems. However, the applications of 3D stacked structures are constrained by the surface deformation of each thin layer induced by thermal effects, vibration, gravity, and other environmental stresses. Therefore, ensuring the performance and reliability of 3D stacked structures necessitates the precise measurement of nanoscale deformation in each layer. Furthermore, the spacing between layers in 3D stacked structures using modern microelectronics and packaging technologies is exceedingly small, making it impossible to measure the deformation of all layers. Here, we present a novel optical endoscope that fuses a miniaturized interferometry array, a laser-fabricated microprobe, and a highly efficient profile reconstruction algorithm for the precise measurements of surface deformation across all layers in 3D stacked structures. Our method offers a potentially effective and noninvasive way to address the challenges associated with in-line deformation measurement across all layers in real 3D stacked wafers and chips.



KEYWORDS: *3D stacked structures, surface deformation metrology, optical endoscope, nanoscale deformation, noninvasive*

INTRODUCTION

Integrated circuits (ICs) are reaching their physical limits as elements on a dense IC can only be so small and tightly packed before they interfere with each other and lose their functionality. To keep Moore's law going, there is a potential paradigm shift toward 3D transformation in chips to sustain continuous improvements in semiconductor device performance and computational speed.[1,2] IC products based on 3D chip stackings are characterized by a high degree of integration, light weight, compact packaging size, and low manufacturing costs. These attributes enable a drastic increase in transistor density, which is promising for further miniaturization, high-density integration, high reliability, and low power consumption.[3−8] Fabricating a 3D stacked chip involves overlaying multiple layers with different functionalities through micromachining and interconnecting processes, such as using Through Silicon Vias (TSV) and Cu pillars.

However, the increase in the number of layers is typically accompanied by the decrease in the thickness of each layer, which amplifies the impact of thermal and gravity effects, as well as environmental stress on the deformation (for example, warping and bending) of 3D stacked structures. As the deformation can significantly reduce the device's lifespan,[9,10] accurate measurement of deformation in 3D stacked structures is essential for predicting the device's performance. Current techniques for measuring surface morphology and deformation include optical interferometry[11] (e.g., laser interferometry,[12,13] white light interferometry (WLI),[14,15] and other methods), laser confocal techniques,[16,17] spectral confocal techniques,[18,19] scanning electron microscopy (SEM),[20,21] atomic force microscopy (AFM),[22,23] and others. However, the spacing in a 3D stacked chip is typically between tens to hundreds of micrometers,[24,25] making it impossible for these traditional top-down surface measurement techniques to measure the deformation across all layers due to the limited penetration depth of photons and electrons. Therefore, there is an urgent need for developing a high-precision, nondestructive, and efficient system to measure the deformation of all layers in 3D stacked structures.

In this work, we present a stacked interferometry array system (SIAS), which consists of an embedded micromirror

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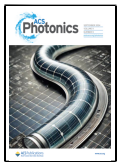

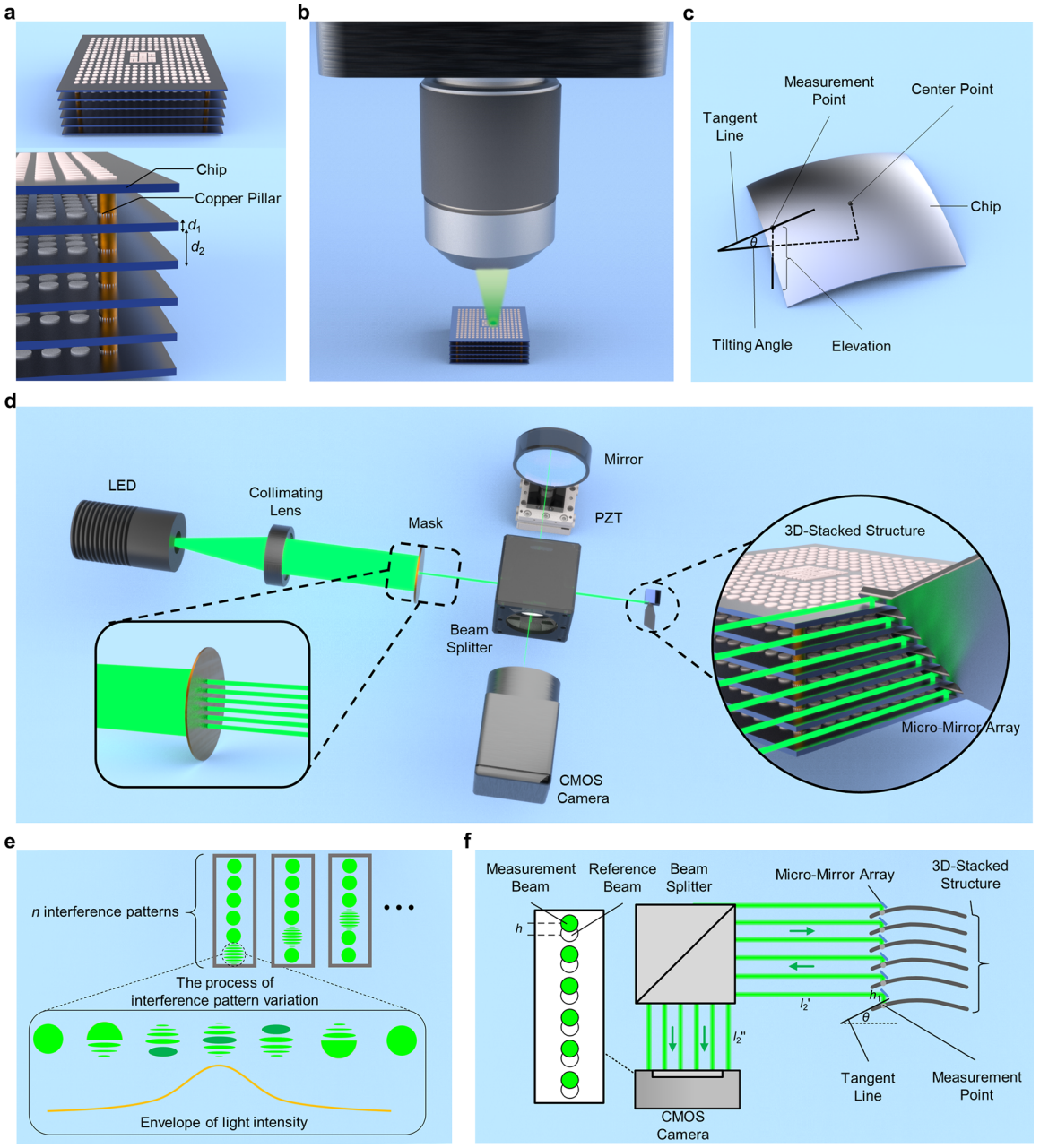

Figure 1. Representative 3D stacked structure and the principle of the SIAS. (a) Schematic diagram of a representative 3D stacked structure with six layers connected by copper pillars. (b) Schematic diagram of a conventional top-down measurement technique. (c) Schematic diagram showing the measurands (i.e., the elevation and tilting angle of a measurement point on a layer of the 3D stacked structure) of our SIAS. (d) Schematic diagram of the SIAS. The mask pattern shown in the lower left corner is a linear array of pinholes with a period of $d_1 + d_2$. The zoomed-in image shown on the right side reveals the position of the 3D stacked structure relative to the micromirror array during the measurement. (e) Schematic diagram showing the elevation measurement process. The upper side shows n types of interference patterns acquired by the camera, where n denotes the number of layers in the 3D stacked structure. The lower side shows the variation of one of the interference patterns during the measurement process. A Gaussian envelope of intensity at the center of the interference pattern can be observed. (f) Schematic diagram showing the tilting angle measurement process. h_1 is the distance between the micromirror and the measurement point on the layer surface. θ is the angle between the tangent line and the measurement point on the 3D stacked structure and the horizontal line. l_2' is the distance between the micromirror and the beam splitter. l_2'' is the distance between the beam splitter and the CMOS camera. h is the center offset of the reflected light in the measurement beam, with respect to that in the reference beam captured by the CMOS camera.

array and a multibeam while-light interferometer, for the precise monitoring of nanoscale deformation of all layers in an in-house fabricated 3D stacked structure. Our experiments demonstrate that the SIAS could measure the deformations of all layers in a 3D stacked structure with nanometer accuracy, which may find applications in large-scale and high-volume manufacturing scenarios, such as integrated circuits and additive manufacturing. We believe that this work not only offers a promising avenue for addressing the challenges associated with the precise deformation measurement for 3D stacked wafers and chips but also paves the way for many other fields where geometrical measurement in micrometer scale spacing is impossible using conventional measurement techniques.

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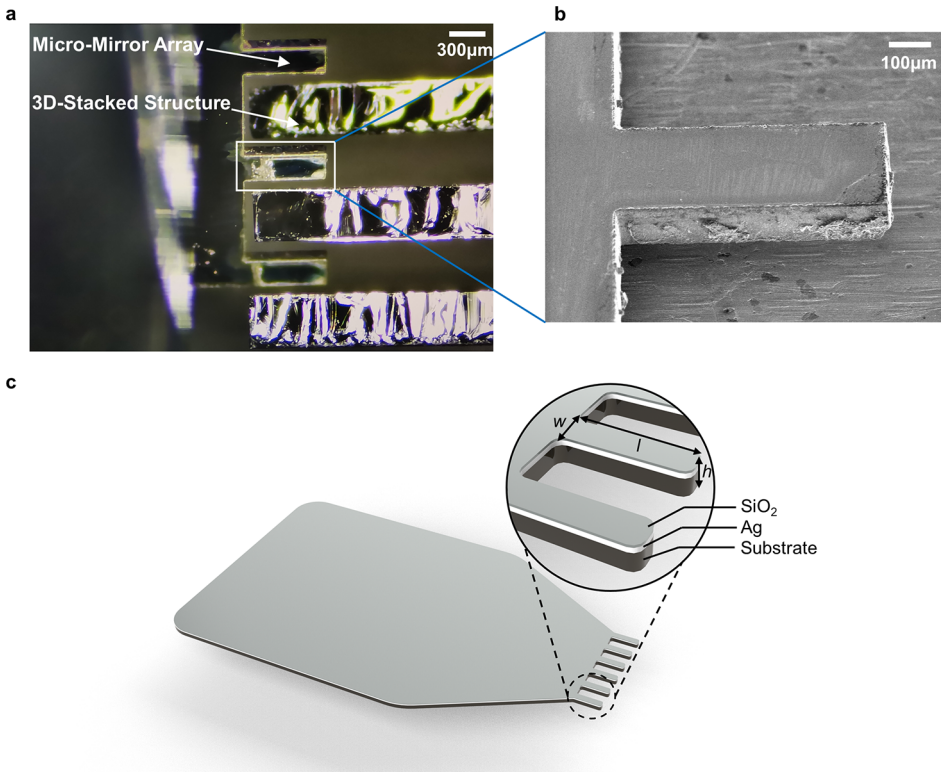

Figure 2. Fabricated micromirror array. (a) Optical image showing the position of the micromirror array relative to the 3D stacked structure in working conditions. The micromirror array was loaded on a fixture on the left (not shown), and the 3D stacked structure was mounted on the right. (b) Scanning electron micrograph of a single micromirror. (c) Schematic diagram of the designed micromirror array.

METHODOLOGY

Measurement System and Deformation Reconstruction Method. In recent years, various studies on 3D stacked structures such as 3D stacked chips have emerged.[26,27] The geometry of a typical 3D stacked structure, as shown in Figure 1a, involves multiple layers of structures at certain intervals along the z-axis, interconnected by copper pillars. In the diagram, d_1 and d_2 represent the thickness of a single layer and the spacing, respectively. The deformation map of a layer in the 3D stacked structure can be obtained by fitting the deformations at multiple measurement points on the layer surface. This method allows rapid measurement of surface deformations across all of the layers in a 3D stacked structure compared to the conventional WLI. The deformation of a measurement point can be fully characterized by the elevation and the tilting angle at this point. The elevation is defined as the height of a measurement point relative to the horizontal plane, and the tilting angle is defined as the angle between the tangent line to the measurement point and the horizontal plane (see the definition of elevation and tilting angle in Figure 1c).

The schematic diagram of the SIAS is illustrated in Figure 1d. We used a fiber-coupled LED with a central wavelength of 530 nm and a bandwidth of 30 nm as the light source (model M530F2; Thorlabs Inc.). The light source is first collimated through a collimating lens, after which the beam passes through a mask for beam splitting before it goes through a beam splitter. The mask is used to split the beam into n sub-beams, where n equals the number of layers in the 3D stacked structure. As a result, n sub-beams passing through the beam splitter are reflected by the micromirror array that is inserted into the 3D stacked structure to illuminate the layer surface vertically. The positioning of the micromirror array is governed by an XYZ movement stage and a side-view microscope (not shown in Figure 1d). The reflected beams from the layer surfaces are reflected by the same micromirror array, after which the beams are collected by a complementary metal oxide semiconductor (CMOS) camera. Another n sub-beam split by the beam splitter is reflected by a high-quality reference mirror followed by being captured by the same CMOS camera. By controlling the piezoelectric transducer (PZT) stage to drive the displacement of the reference mirror, the optical path difference of the two sets of sub-beams can be adjusted, thus generating n interference patterns in the CMOS camera (see the schematic of n interference patterns in a frame in the inset of Figure 1e).

To measure the elevation, WLI is introduced. By controlling the PZT stage to drive the displacement of the reference mirror, the optical path difference between the reference beam and the measurement beam can be adjusted. During this process, the variation of the interference pattern captured by the CMOS camera is schematically shown in Figure 1e. The light intensity at the center of the interference pattern is maximum when the optical paths of the reference and measurement beams are equal. The phase-shifting algorithm[29] can be used to process the interference pattern to obtain an accurate value of the current position (noted as a_2) of the PZT stage (see more details in the Supporting Information). The initial position of the PZT is noted as a_1, and then, the distance between a_1 and a_2 is the elevation of the measurement point. To measure the tilting angle at the measurement point, we obtain the positions of the reference beam and the measurement beam in the CMOS camera separately. Here, the position of a beam is defined as the coordinates of the center of the beam. The center offset between the reference beam and the

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measurement beam reflects the magnitude of the tilting angle of the measurement point (see the schematic in Figure 1f). Based on the geometric relation of the propagation path of the measurement beam, the tilting angle of the measurement point can be calculated approximately. Figure 1f shows the schematic diagram of the measurement process of the tilting angle at a measurement point. The calculation of the tilting angle of the measurement point can be expressed as $\theta = \frac{1}{2}\arctan\left(\frac{2h - \sqrt{2}l_1}{2l_2 - \sqrt{2}l_1}\right)$, where θ is the tilting angle of the measurement points on the layer surface, h is the center offset between the measurement beam and the reference beam captured by the CMOS camera, l_1 is given by $l_1 = h_1 \sin 2\theta / \sin\left(\frac{\pi}{4} - 2\theta\right)$, where h_1 is the distance from the position where the beam enters the micromirror array to the measurement point on the 3D stacked structure, and l_2 is the sum of distances between the CMOS camera and the micromirror array, i.e., $l_2 = l_2' + l_2''$, as shown in Figure 1f. In contrast to traditional top-down surface measurement techniques (see Figure 1b), our measurement system (i.e., SIAS) could achieve direct monitoring of the nanoscale deformation of all layers in a 3D stacked structure in a fast and nondestructive mode.

As shown in Figure 1d, the mask pattern is designed as a vertically arranged circular pinhole array with a period of $d_1 + d_2$, where d_1 and d_2 equal the thickness of a single layer and the spacing in the chip, respectively. The function of the mask is to split the collimated beam into multiple parallel beams at the preset spacing (i.e., $d_1 + d_2$). For the diameter of the pinhole on the mask larger than approximately 2λ and the thickness of the Cr layer on the mask less than approximately 0.5λ (where λ denotes the wavelength of the light source), diffraction effects can be neglected.[28] Therefore, the size of the pinholes on the mask can be as small as 1 μm. The function of the micromirror array is to reflect the parallel beam passing through the beam splitter followed by illuminating the surface of each layer vertically. The reflected beam from each layer is then reflected by the same micromirror array. The geometrical structure of the micromirror array, as shown in Figure 2c, has a large and planar area on the left for the purpose of clamping and easy installation at a 45° angle in the SIAS, while the comb-like geometry on the right-hand side functions as a mirror array to be inserted into the 3D stacked structure for bending the propagation direction of the sub-beam array. The period, thickness, width, and length of the comb-like geometry are $d_1 + d_2$, h, w, and l, respectively. The micromirror array is fabricated on a silicon substrate with a polished surface, covered with a 0.2 μm silver film and a 0.1 μm silicon dioxide protective film. The relationship between the spacing d_2 of 3D stacked structures, the probe thickness h, and the design width w is given by $d_2 = \sqrt{2}w + (h + 0.3 - w)/\sqrt{2}$. If the micromirror array is fabricated using a commercially available silicon substrate with a thickness h of 20 μm and a design width w that can receive a beam diameter of 10 μm, then the smallest spacing d_2 that the SIAS can be applied is approximately 24.4 μm. Figure 2a shows the position of the micromirror array relative to the 3D stacked structure in working conditions, and the SEM image of the fabricated micromirror array is shown in Figure 2b. The PZT stage used in our system has a built-in Si-HR sensor for feedback. Its motion stage travel is 100 μm, and its closed-loop resolution is 0.1 nm, with 0.02% linearity and 0.2 nm repeatability. The longitudinal resolving power of the measurement system is better than 1 nm. The resolution, pixel size, and frame rate of the monochrome CMOS camera used in the system are 1936 × 1216, 5.86 μm, and 155 fps, respectively. The system architecture also encompasses a measurement auxiliary motion system for clamping and moving the micromirror array, a side-viewing microscope for micromirror array alignment, and a system support structure for reducing the environmental vibration (not shown in Figure 1; see more details in the Supporting Information). The designed micromirror array is affixed to an *XYZ*-axis platform, facilitating easy adjustments and replacements. The 3D stacked structure under test is positioned on a multidegree-of-freedom pose adjustment platform for configuring the measurement pose. This mechanism comprises electrically controlled *XY*-axis and rotary platforms. A horizontal microscope is employed to observe the positions of the micromirror array and the tested 3D stacked structure. The measurement system is placed on a passive air-floating platform to mitigate the impact of environmental vibrations.

RESULTS AND DISCUSSION

Wafer Deformation Monitoring. To validate the capability of the SIAS in deformation measurements, we placed a wafer on a platform that consists of a *z*-axis displacement stage and a rotary stage. By adjusting the linear stage and rotary stage, we can mimic the scenario where a chip or wafer has different levels of deformation. The movement of the *z*-axis displacement stage allows us to capture the elevation information on the measurement points at each step. The step size of the *z*-axis displacement stage was set to 1 μm/step. Additionally, we conducted the measurements at different tilting angles (see the definition of the tilting angle in Figure 3a) implemented by the rotary stage. The step size for the tilting angle was set to 0.01°/step. Here, we should mention that the tilting angle should be small enough that we can measure the change of height instead of the change of the angle. Fortunately, the deformation of a layer in an actual 3D stacked structure (e.g., the 3D stacked chip) is relatively small, which automatically satisfies the assumption of small

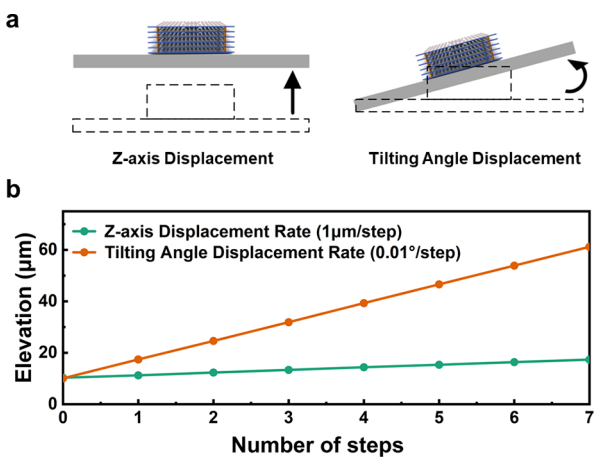

Figure 3. Monitoring of surface deformation. (a) Schematic diagram showing the definition of the *z*-axis displacement error and the tilting angle displacement error. (b) Measured elevation as a function of displacements when linear (the green line) and rotary (the orange line) displacements are introduced.

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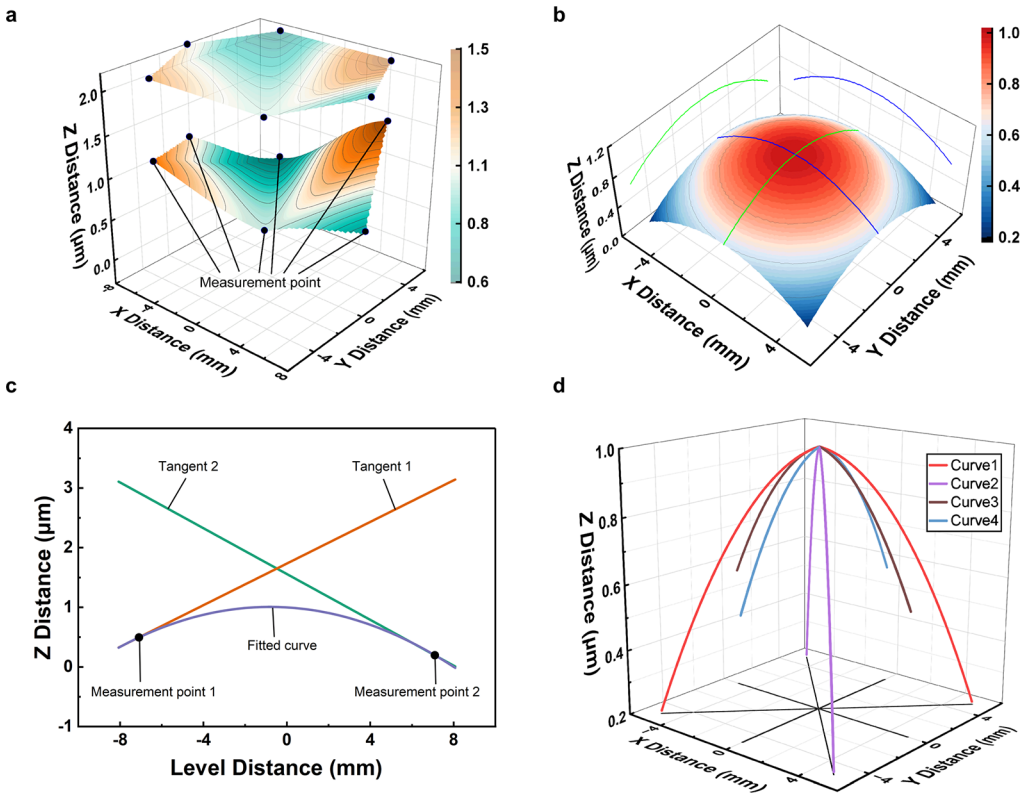

Figure 4. Measurement results of a 3D stacked structure that has deformation in multiple layers. (a) Reconstructed deformation surfaces fitted by the measured elevation at the measurement points. (b) Reconstructed deformation surface fitted by the elevation and tilting angle at the measurement points. (c) Deformation curves fitted to data from two measurement points. "Measurement point 1" and "Measurement point 2" are symmetrical to the center of the chip. The "Fitted curve" is tangent to "Tangent 1" and "Tangent 2" at "Measurement point 1" and "Measurement point 2", respectively. (d) Assembly of all the fitted quadratic curves (i.e., "Curve1", "Curve2", "Curve3", and "Curve4").

deformation. As shown in Figure 3b, the fitted curves present a high degree of linearity, indicating that our measurement system could accurately reconstruct the surface deformation. We should mention that there are still small errors between the measured values and the theoretical ones, which mainly arise from the positioning error of the *z*-axis and rotary stages as well as the environmental vibration. Here, we should emphasize that the *z*-axis and rotary stages are only used to mimic the deformation of the chip and are not included in the SIAS. Therefore, the positioning errors of the *z*-axis and rotary stages do not affect the measurement results of the 3D stacked structures below.

Deformation Measurement for 3D Stacked Structures. To obtain the deformation distribution of each layer in a 3D stacked structure, the SIAS was employed to measure deformations at multiple points on each layer of the 3D stacked structure. These points are chosen in such a manner that they distribute uniformly around the center of the 3D stacked structure. If the tilting angle of the measurement points is negligible, then the cubic spline interpolation (CSI) method[30] is applied to fit the elevation of these measurement points to obtain the deformation distribution of the chip. CSI involves approximating the surface with a cubic polynomial near each point. This ensures that the smoothness of the interpolation results in the vicinity of the data points and adapts to the variations in the data using local information. The resulting deformation distribution of a layer is depicted in Figure 4a, in which we are able to observe the overall deformation of the chip as well as the height and coordinate data of individual points on the layer surface (the geometrical center of the bottom layer of the 3D stacked structure is defined as the origin of the Cartesian coordinate system). These data provide a comprehensive understanding of the deformation of the chip. The chip exhibits curvature variations that reveal possible bending in its structure. To be more specific, the chip has a maximum curvature of 1.837×10^{-4} μm^{-1} at the point (0.62 mm, 4 mm). If the tilting angle of the measurement point is not negligible, then the fitting of the deformation distribution of the chip involves several steps. First, two measurement points symmetrical to the center of the chip are selected as a combination, such as "Measurement point 1" and "Measurement point 2" in Figure 4c. The elevation and tilting angles at the two measurement points can be formed into two straight lines as "Tangent 1" and "Tangent 2", respectively. A curve named "Fitted curve" is then fitted using the polynomial fitting method.[31] The "Fitted curve" is tangent to "Tangent 1" and "Tangent 2" at "Measurement point 1" and "Measurement point 2", respectively. Subsequently, the quadratic curves obtained from all combinations of measurement points are assembled into the same three-dimensional space, as depicted in Figure 4d. "Curve1", "Curve2", "Curve3", and "Curve4" represent different quadratic curves formed by various combinations of measurement points. Finally, the three-dimensional surface is fitted using the quadratic curve based on the method of cubic polynomial surface fitting[31] (see Figure 4b). As shown in Figure 4b, we can observe the details of the curvature and bump deformation on each layer. The whole structure has a center convex deformation with a maximum height difference of 0.79 μm.

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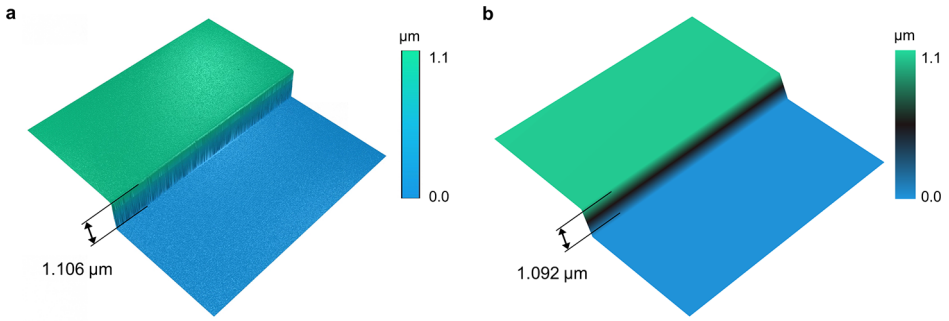

Figure 5. Measured deformation distribution of a step specimen. The measurement results of surface deformation were obtained using (a) the commercial WLI ER230 and (b) SIAS.

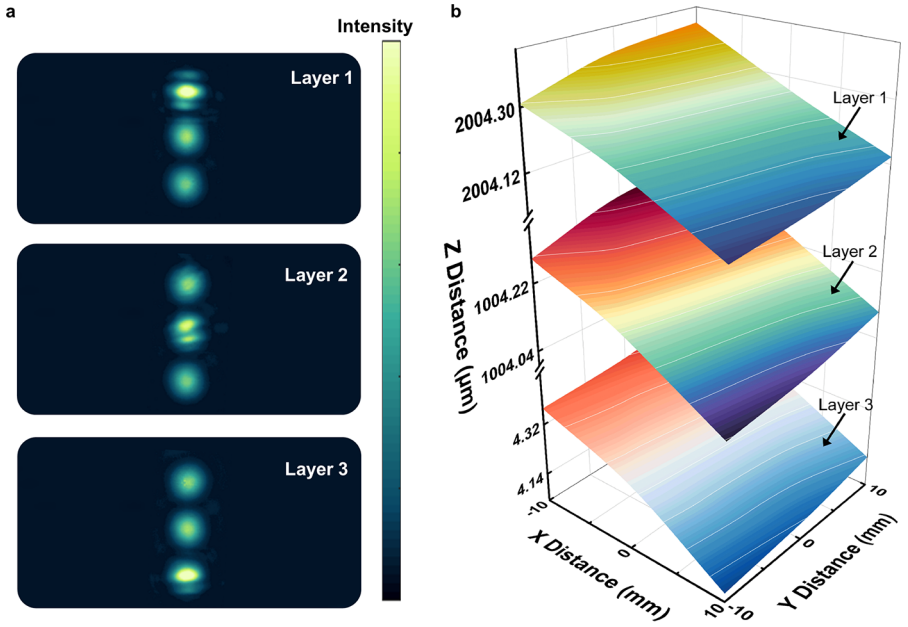

Figure 6. Measured deformation distribution of a 3D stacked structure. (a) Raw measurement signal. A partial interference pattern was acquired by the CMOS camera during a single measurement by the measurement system, which represents the interference pattern for each layer separately. (b) Measurement results of three layers in the stacked structure.

Moreover, there is a maximum curvature of 4.98×10^{-3} μm^{-1} at the origin.

We evaluated the performance of the SIAS by measuring the surface deformation of an in-house fabricated step specimen, which is made by depositing a layer of aluminum film (1.1 μm thick) on half of the surface of a silicon wafer using electron beam evaporation (EBE) technology. The surface deformation on the step specimen was first measured by a commercial WLI (model ER230; Atometrics, Inc.) with a 0.4 NA objective (Figure 5a). The deformation area that could be measured using the commercial WLI is about 400 μm wide by 400 μm long due to the limited field of view. We then compared the measured results from the commercial WLI to those from the SIAS. We used the measurement results from ER230 with a 0.4 NA objective as the golden standard for the comparison. As shown in Figure 5a,b, the step heights measured by ER230 and SIAS are 1.106 and 1.092 μm, respectively. The 14 nm difference demonstrates that the SIAS is capable of achieving accurate measurements for surface profile and deformation.

The 3D stacked structure under test consists of three layers, whose sizes are d_1 = 500 μm and d_2 = 500 μm (see the definition of d_1 and d_2 again in Figure 1a). To make the measurement of the 3D stacked structure feasible, the period of the mask's pinhole array should be the same as the period of the 3D stacked structure, and the pinhole diameter of the mask should be less than d_2. Therefore, the periodicity of the pinhole array mask was set at 1 mm with a pinhole diameter of 200 μm. The parameters of the micromirror array used in our measurement system were 1 mm periodicity, h = 150 μm, w = 283 μm, and l = 680 μm (see Figure 2c). Some interference patterns acquired by the CMOS camera during the measurement of the three-layer structure by the SIAS are shown in Figure 6a, where each image contains the interference patterns of three layers of the 3D stacked structure. The three CMOS camera images in Figure 6a show distinct interference fringes for each layer of the 3D stacked structure. The measured deformation results for the three-layer structure are presented in Figure 6b, in which we can observe the details of the deformation distribution of each layer. The maximum differences in elevation of the layers from top to bottom are 0.3411, 0.3347, and 0.3972 μm, respectively. The maximum curvatures of all layers from top to bottom are 1.51×10^{-5} μm^{-1} at position (0.36 mm, −0.28 mm), 1.6×10^{-5} μm^{-1} at position (−0.08 mm, 0.38 mm), and 2.11×10^{-5} μm^{-1} at position (−0.7 mm, 0.7 mm). These data demonstrate that our

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measurement system could measure the nanometer-scale deformation of multilayer structures simultaneously.

CONCLUSIONS

This study introduces an innovative method named the stacked interferometry array system for the precise monitoring of the surface deformation of all layers in a 3D stacked structure. We experimentally demonstrated that the measurement accuracy of our system could reach the nanometer scale, and the measurement time for a single measurement point is less than 10 s after the measurement system was calibrated. The accuracy and speed of measurement can be further improved by using a high-precision and fast PZT stage alongside a careful calibration of the measuring system. Moreover, it is expected that the system can also be utilized to measure the nanoscale deformation of multiple layers in a 3D stacked structure with even smaller spacing (e.g., < 10 μm) by using a smaller micromirror array that can be fabricated through a standard semiconductor fabrication process. We hope that this work could not only address current challenges of in-line or *in situ* deformation monitoring of all layers in 3D stacked chips in the fab but also may pave the way for many other fields where deformation or dimension measurement in micrometer scale spacing is impossible using conventional top-down measurement techniques.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.4c00784.

The experimental system for 3D stacked structure measurement; design and fabrication of the micromirror array; extraction of interference patterns for each layer in a 3D stacked structure; calculation of the elevation distribution (PDF)

AUTHOR INFORMATION

Corresponding Authors

Jinlong Zhu − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China; Research Institute of Huazhong University of Science and Technology Shenzhen, Shenzhen 518057, China; Optics Valley Laboratory, Wuhan, Hubei 430074, China;* orcid.org/0000-0002-5723-2879; Email: jinlongzhu03@hust.edu.cn

Shiyuan Liu − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China; Optics Valley Laboratory, Wuhan, Hubei 430074, China;* orcid.org/0000-0002-0756-1439; Email: shyliu@hust.edu.cn

Authors

Xiangyu Zhao − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China;* orcid.org/0009-0003-7844-1922

Hao Jiang − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China; Optics Valley Laboratory, Wuhan, Hubei 430074, China;* orcid.org/0000-0003-0561-5058

Jiamin Liu − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China*

Changqing Liu − *State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China*

Hui Deng − *Department of Mechanical and Energy Engineering, Southern University of Science and Technology, Shenzhen, Guangdong 518055, China;* orcid.org/0000-0002-7116-7188

Renjie Zhou − *Department of Biomedical Engineering, The Chinese University of Hong Kong, Hong Kong, China;* orcid.org/0000-0002-4761-6641

Nicholas X. Fang − *Department of Mechanical Engineering, University of Hong Kong, Hong Kong, China*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsphotonics.4c00784

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Notes

The authors declare the following competing financial interest(s): The authors claim a C.N. patent and a U.S. patent on the presented method in this work through Huazhong University of Science and Technology.

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Supporting Information

Direct monitoring of nanoscale deformations across all layers in 3D-stacked structures

Xiangyu Zhao[1], Hao Jiang[1,3], Jiamin Liu[1], Changqing Liu[1], Hui Deng[4], Renjie Zhou[5], Nicholas X. Fang[6], Shiyuan Liu[1,3], and Jinlong Zhu[1,2,3*]

[1]State Key Laboratory of Intelligent Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China
[2]Research Institute of Huazhong University of Science and Technology Shenzhen, Shenzhen 518057, China
[3]Optics Valley Laboratory, Wuhan, Hubei 430074, China
[4]Department of Mechanical and Energy Engineering, Southern University of Science and Technology, No. 1088, Xueyuan Road, Shenzhen, Guangdong 518055, China
[5]Department of Biomedical Engineering, The Chinese University of Hong Kong, Shatin, New Territories, Hong Kong, China
[6]Department of Mechanical Engineering, University of Hong Kong, Hong Kong, China

*Corresponding author: jinlongzhu03@hust.edu.cn and shyliu@hust.edu.cn

Contents:

S1. The experimental system for 3D-stacked structure measurement

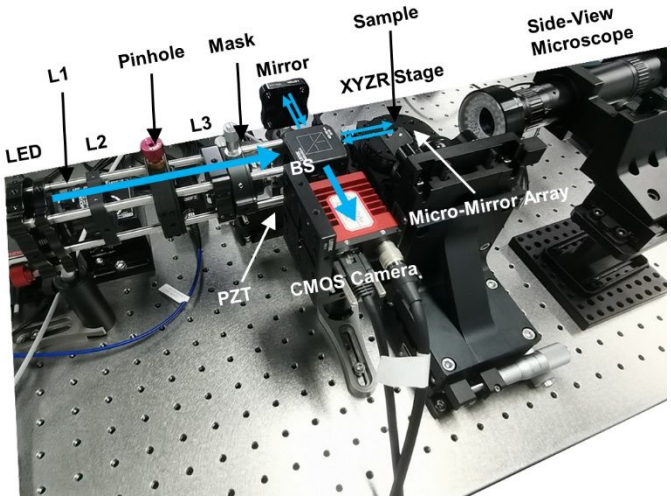

Figure S1 The experimental system for 3D-stacked structure measurement.

The experimental system for measuring the surface deformation of 3D-stacked structures is illustrated in Figure S1. The experimental apparatus employs an LED light source with a central wavelength of 530 nm, which is collimated by a collimating lens (L1). The pinhole filtering module consists of a convex lens (L2) with a focal length of 50 mm, a pinhole with a diameter of 100 μm, and an additional convex lens (L3) with a focal length of 30 mm. The beam is split into *n* sub-beams by the mask after passing through the pinhole filter. One portion of the optical beam is directed towards the micro-mirror array, which is inserted into the stacked structure to bend the beam and illuminate the inner layers of the structure, while the other portion is incident on a reference mirror attached to a PZT. The reflected beams from two paths are captured by the same CMOS camera. The experimental apparatus is placed on a passive air-floatation platform, with the micro-mirror array fixed on an XYZ-axis stage and the 3D-stacked structure positioned on a four-axis XYZR displacement stage. The positions of the micro-mirror array and the tested 3D-stacked structure can be observed through a side-view microscope.

S2. Design and fabrication of the micro-mirror array

The micro-mirror array was fabricated using a silicon flake as a substrate with a polished surface. The substrate was processed to a desired shape and size using femtosecond laser machining. The substrate is then rinsed with deionized water to remove impurities from the substrate surface and dried with nitrogen. To ensure a high reflectance for a broadband wavelength range, a 200 nm-thick silver film was deposited on the surface using electron beam evaporation (EBE) technology. Silver was chosen because its reflectance exceedes 95% in the visible range. Silver tends to react with sulfides in the air over time, which may reduce its reflectance over time. To prevent this, a 100 nm-thick silicon dioxide protective film was grown on the silver film using plasma-enhanced chemical vapor deposition (PECVD) technology.

S3. Extraction of interference patterns for each layer in a 3D-stacked structure

The interference patterns of all layers of the 3D-stacked structure are acquired simultaneously in the CMOS camera. Due to the small diameter of the light beam, the interference patterns are not easy to observe. We employ threshold segmentation and Otsu's binarization method to automatically extract the measurement information for each layer to facilitate subsequent data processing.

Image segmentation divides an image into different regions or objects. Threshold segmentation and Otsu's binarization method are commonly used automatic image segmentation techniques[1,2]. The threshold segmentation method classifies pixels into different classes based on the differences in grayscale values between the target objects and the background. By comparing the features of each pixel in the image with the threshold, we can determine whether the pixel belongs to the target region or not. This method transforms a grayscale image into a binary image, i.e. $f(x,y)=\begin{cases}1, f(x,y)\geq H\\ 0, f(x,y)<H\end{cases}$, where $f(x,y)$ is the original image and H is the threshold. The threshold segmentation method obtains non-overlapping regions based on closed connected boundaries. The better the contrast between the target and background images, the more effective the segmentation results. A key technique of this method is the selection of the optimal threshold. Therefore, Otsu's binarization method is employed here to achieve adaptive threshold selection. Otsu's binarization method is based on the maximum between-class variance approach, aiming to find a threshold that maximizes the between-class variance between foreground and background to achieve optimal image segmentation. For each possible threshold H, the image is divided into two categories: *C1* (pixels less than H) and *C2* (pixels greater than or equal to H). The computation of the intra-class variance for both categories is expressed as $w_1\sigma_1^2+w_2\sigma_2^2$, where w_1 is the proportion of pixels in category *C1* to the total number of pixels, w_2 is the proportion of pixels in category *C2* to the total number of pixels, σ_1^2 is the grayscale variance of category *C1*, and σ_2^2 is the grayscale variance of category *C2*. The inter-class variance, representing

the difference between the two categories, is given by $w_1 w_2 (\mu_1 - \mu_2)^2$, where μ_1 and μ_2 are the average grayscale values of categories *C1* and *C2*, respectively. Otsu's binarization method aims to find a threshold *h* that maximizes the between-class variance, i.e. $h = \arg max\left[w_1 w_2 (\mu_1 - \mu_2)^2 \right]$. Once the threshold corresponding to the maximum between-class variance is determined, the image is divided into two categories: pixels below *h* belong to one category, while pixels greater than or equal to *h* belong to the other category. The interference information for each layer in the 3D-stacked structure can be obtained separately by using the threshold segmentation method and Otsu's binarization technique.

S4. Calculation of the elevation distribution

A phase-shifting algorithm[3] is employed to process the interference pattern for obtaining the elevation, after obtaining the interference pattern for each layer of the 3D-stacked structure. The phase shift algorithm is based on the principle of white light interferometry. It calculates the phase of the peak point by introducing a phase shift. Subsequently, the surface height is computed using the known parameters (including the center wavelength of the light source and the step distance of the PZT stage) of light source and PZT stage. In this study, a four-step phase-shifting method is utilized. The intensity of light at the center of the interference pattern can be expressed as

$$I = 2\times\sqrt{I_r \times I_m}\times\cos\varphi + I_r + I_m + \varepsilon_1, \tag{1}$$

where I_r and I_m are the intensities of the reference and measurement beams, respectively. φ is the phase difference between the reference beam and the measurement beam. ε_1 is environmental noise. In Equation (1), I_r and I_m are constants, ε_1 is approximately constant, so Equation (1) can be expressed as

$$I = A\cos\varphi + B, \tag{2}$$

where $A = 2\times\sqrt{I_r \times I_m}$ and $B = I_r + I_m + \varepsilon_1$. The step distance of the PZT stage set during the measurement is $\lambda/8$ (λ is the center wavelength of the light source), then the phase difference between two adjacent interference patterns is $\pi/2$, and the intensity expression for four consecutive interference patterns in one cycle is

$$\begin{aligned} I_1 &= A\cos\varphi + B \\ I_2 &= A\cos\left(\varphi + \frac{\pi}{2}\right) + B = -A\sin\varphi + B \\ I_3 &= A\cos\left(\varphi + \pi\right) + B = -A\cos\varphi + B \\ I_4 &= A\cos\left(\varphi + \frac{3\pi}{2}\right) + B = A\sin\varphi + B. \end{aligned} \tag{3}$$

We then calculate the difference pattern I_1'/I_2' by calculating the difference between I_1/I_2 and I_3/I_4. See the equations below

$$\begin{aligned} I_1' &= I_1 - I_3 = 2A\cos\varphi \\ I_2' &= I_4 - I_2 = 2A\sin\varphi. \end{aligned} \tag{4}$$

Equation (4) can be solved to obtain the phase difference between the reference beam and the measurement beam, i.e., $\varphi = \arctan\left(\frac{I_2'}{I_1'}\right)$. Finally the elevation at the location of the center of the interference pattern can be obtained, i.e., $H_1 = d\left(V - \frac{2\varphi}{\pi}\right)$, where H_1 is the elevation at the center of the interference pattern, d is the step distance of the PZT stage, $d = \lambda / 8$ (λ is the center wavelength of the light source), and V is the coordinate of the PZT stage when the light intensity is maximum at the center of the interference pattern.

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